

ZZZ
DAZ@
DAZ08400100
KAV60 LA-5141P LS-5141P/5142P/5143P

ZZZ
DA2@
DA60000BO10
LA-5141P REV1 M/B

ZZZ
DA2@
DA20000FM10
LS-5141P REV1 PWR/B

ZZZ
DA2@
DA60000BU10
LS-5142P REV1 SDIO/B

ZZZ
DA2@
DA60000BT10
LS-5143P REV1 CARDREADER/B

Compal Confidential

KAV60 Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

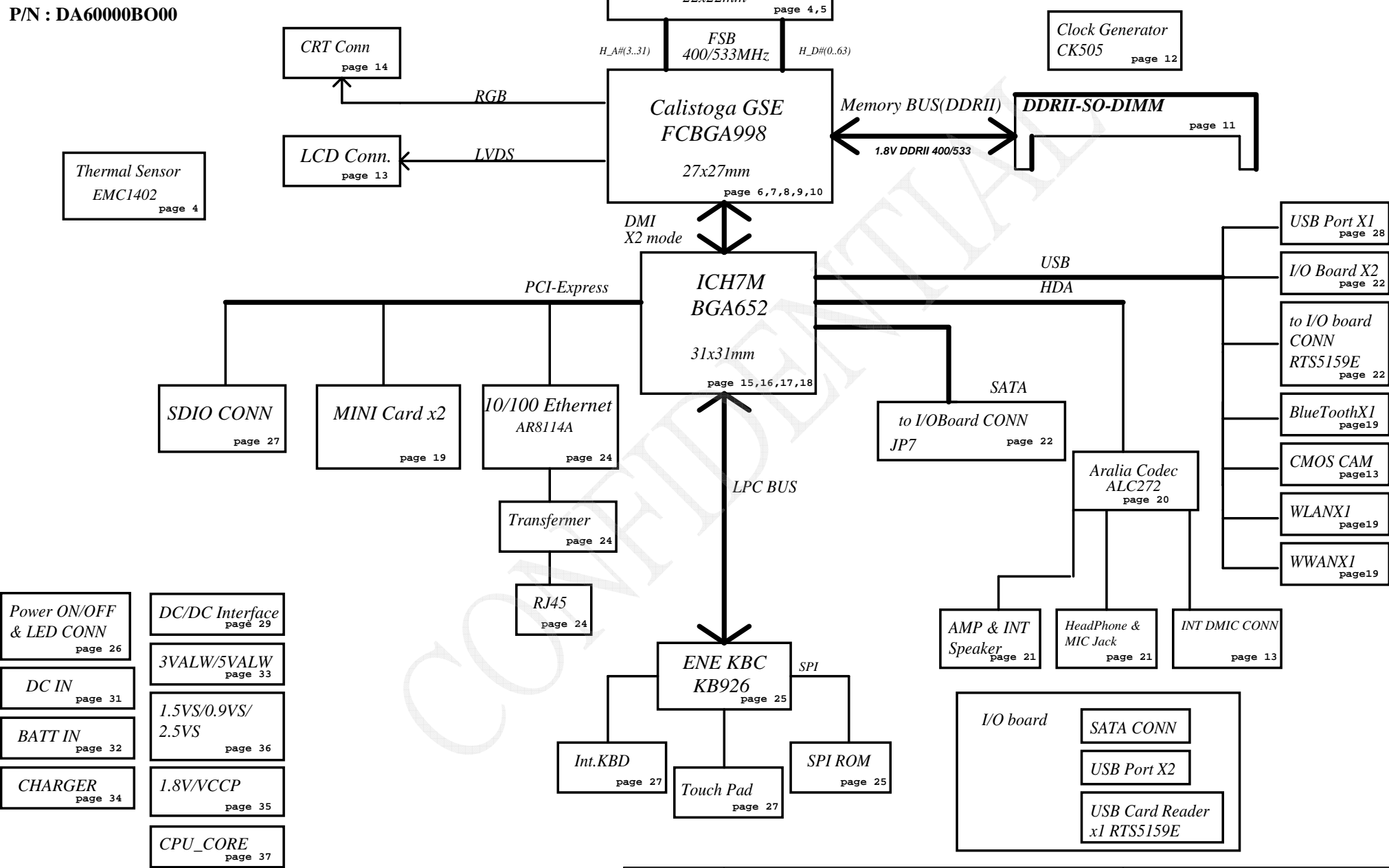
2009-03-06

REV: 1.0

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Compal Confidential

Model Name : KAV60
File Name : LA-5141P
P/N : DA60000BO00



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

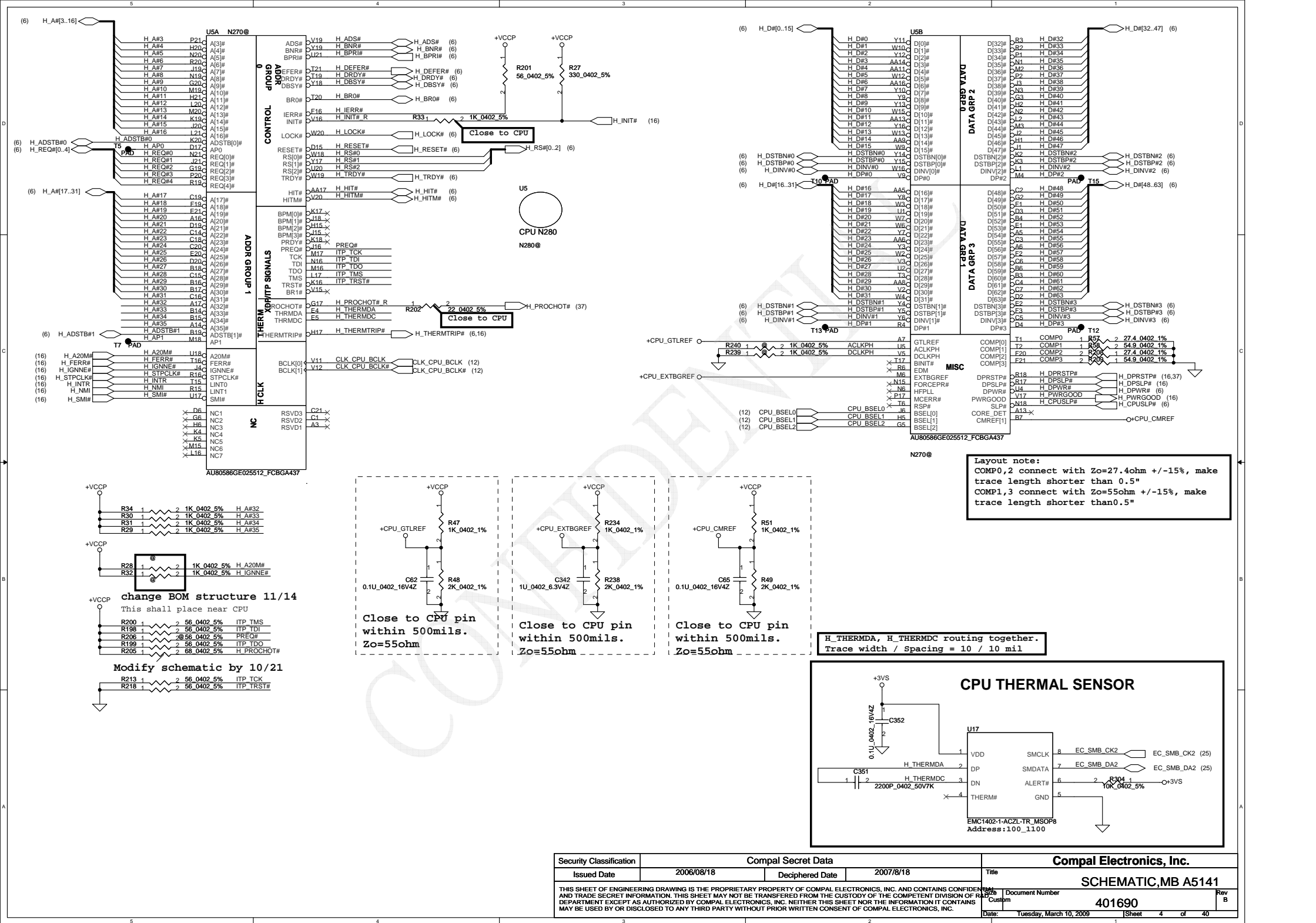
Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

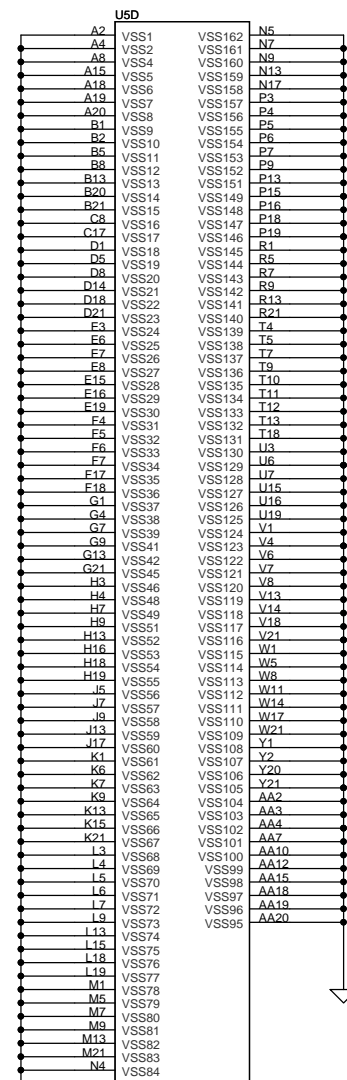
EC SM Bus2 address

Device	Address
EMC1402	1001 100X b

ICH7M SM Bus address

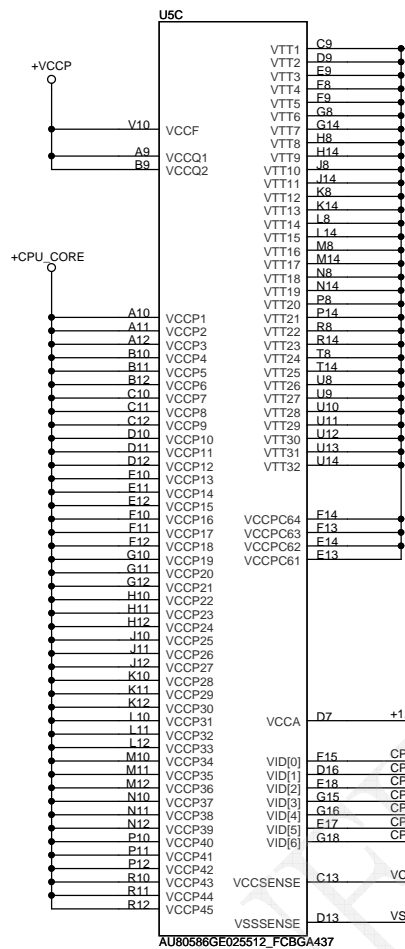
Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb





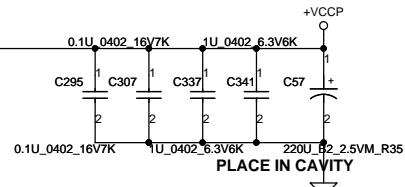
AU80586GE025512_FCBGA437

N270@

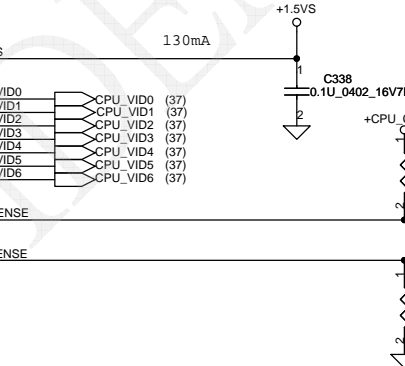


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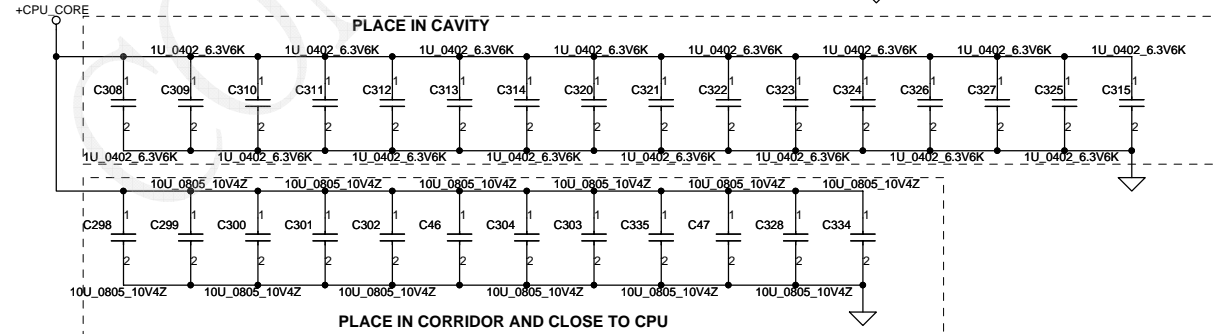
N270@



PLACE IN CAVITY

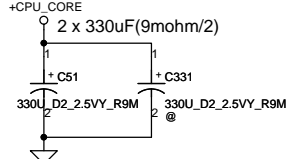


Length match within 25 mils
The trace space 7 mils,
Zo=27.4ohm

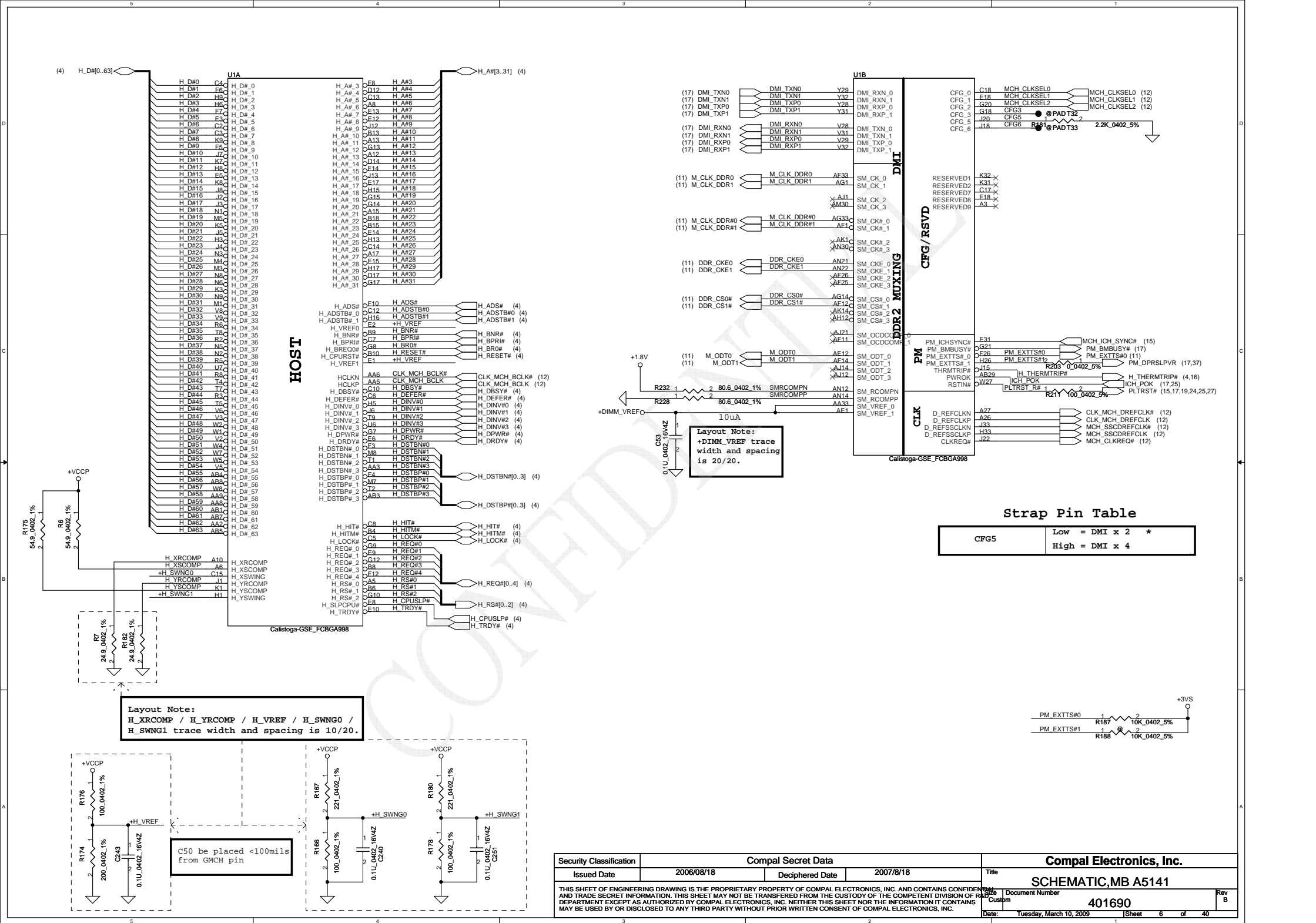


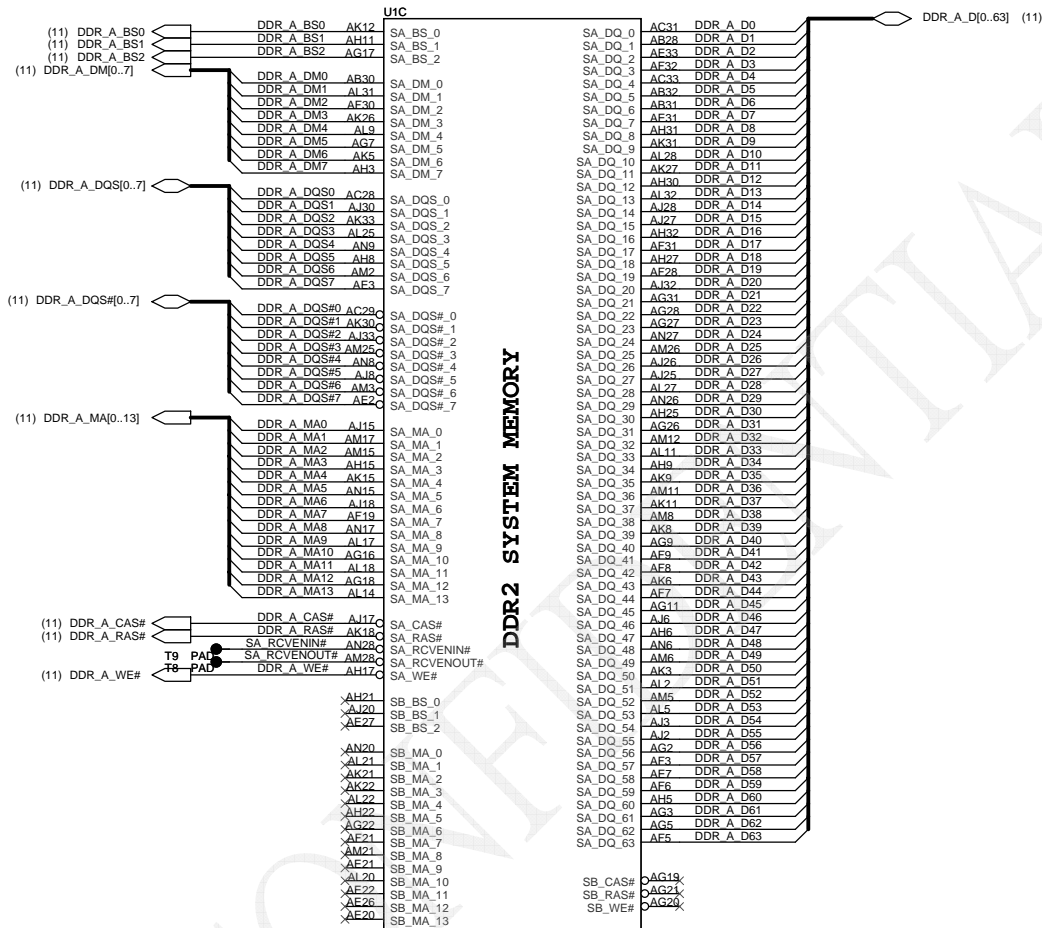
PLACE IN CAVITY

PLACE IN CORRIDOR AND CLOSE TO CPU



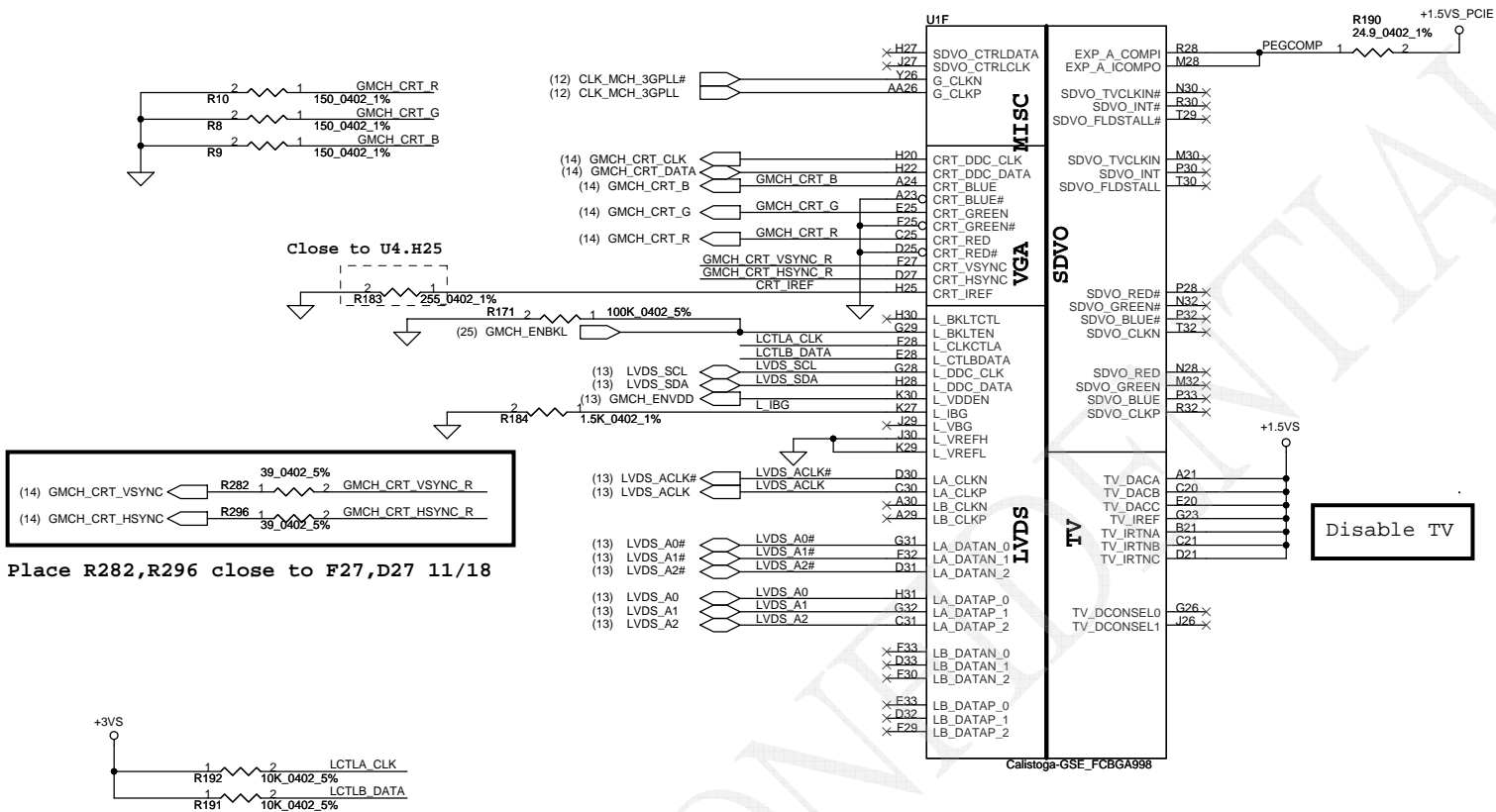
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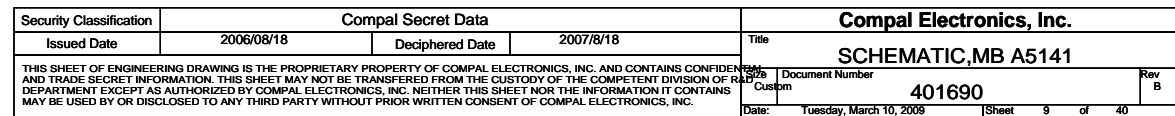


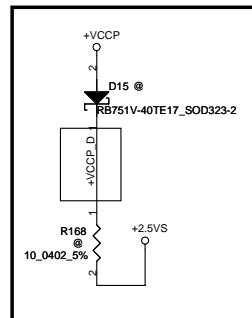
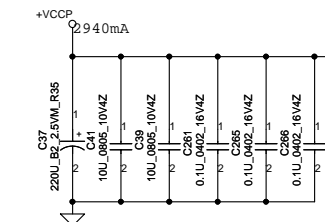
Calistoga-GSE_FCBGA998

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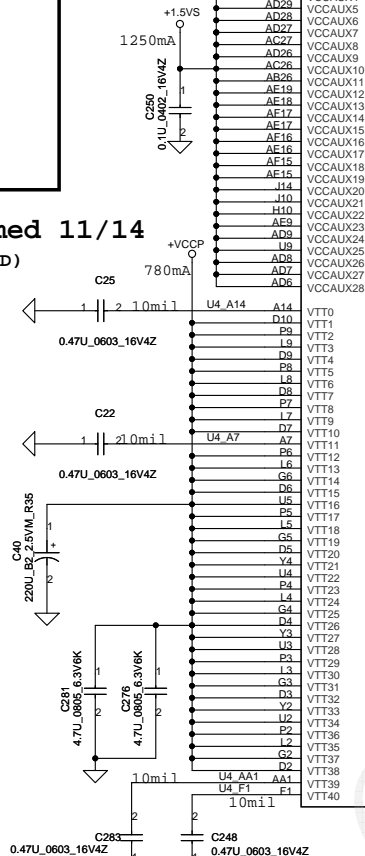


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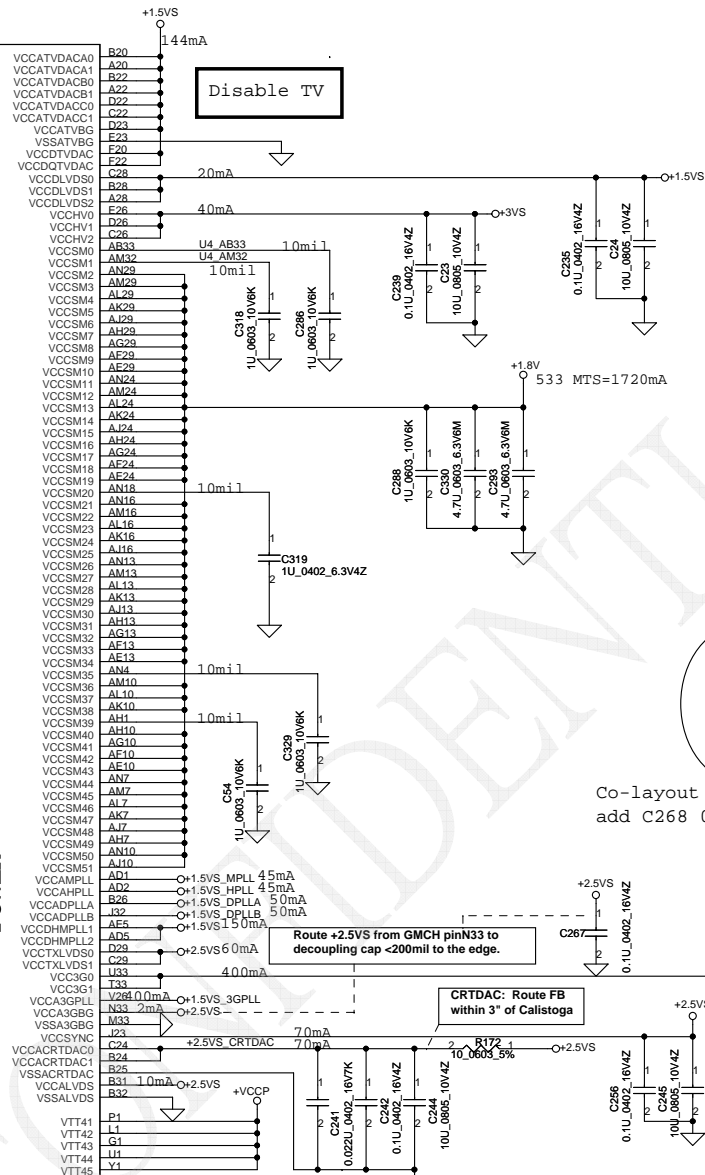


To be confirmed 11/14
add net name(+VCCP_D)
20mil 12/10



POWER

Calistoga-GSE_FCBGA998

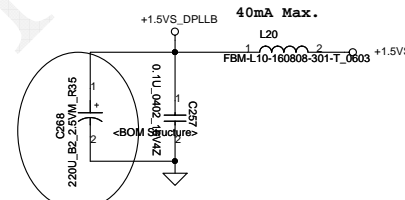
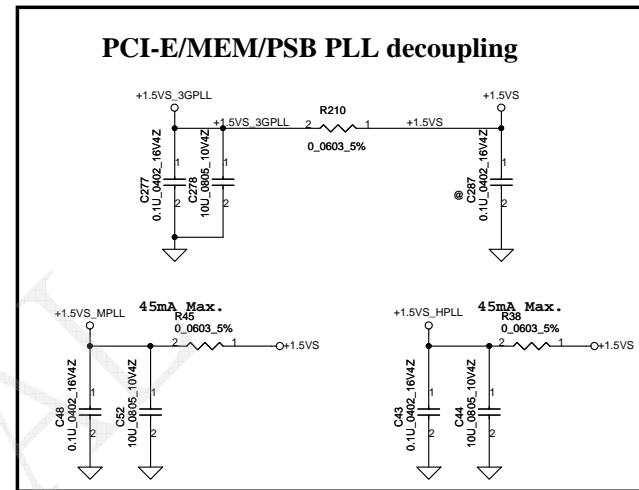


Disable TV

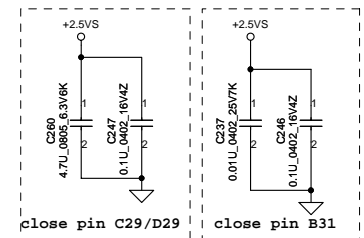
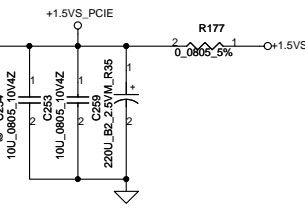
Route +2.5VS from GMCH pinN33 to decoupling cap <200mil to the edge.

CRTDAC: Route FB within 3" of Calistoga

Route VSSACRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.



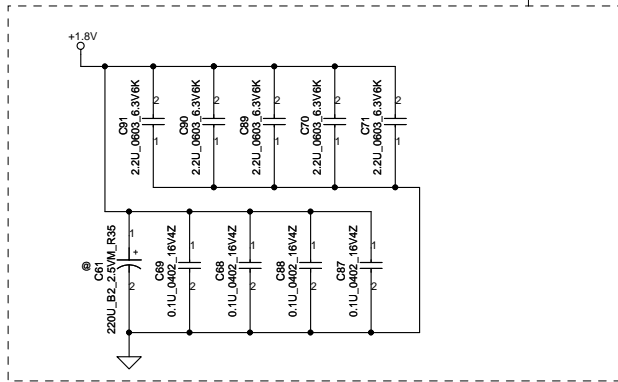
Co-layout with C249 change C249 BOM structure(@) 01/23
add C268 01/22 Del C249 02/18



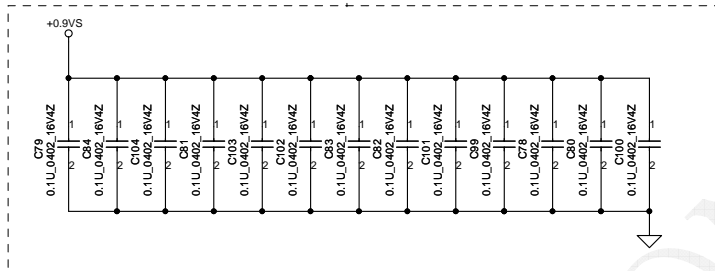
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- (7) DDR_A_DQS#[0..7]
- (7) DDR_A_D[0..63]
- (7) DDR_A_DM[0..7]
- (7) DDR_A_DQS[0..7]
- (7) DDR_A_MA[0..13]

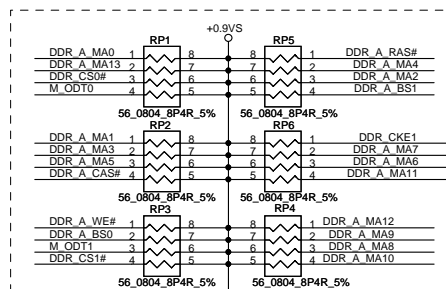
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



add JDIM1 pin 200 and pin 201 to GND
01/20



return the H5.2 footprint 11/24

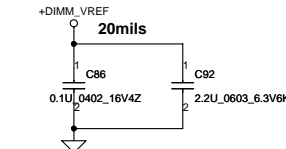
Layout Note:
Place these resistor
closely DIMMA, all
trace length < 750 mil



change DIMMA from H5.2 to H4 11/17

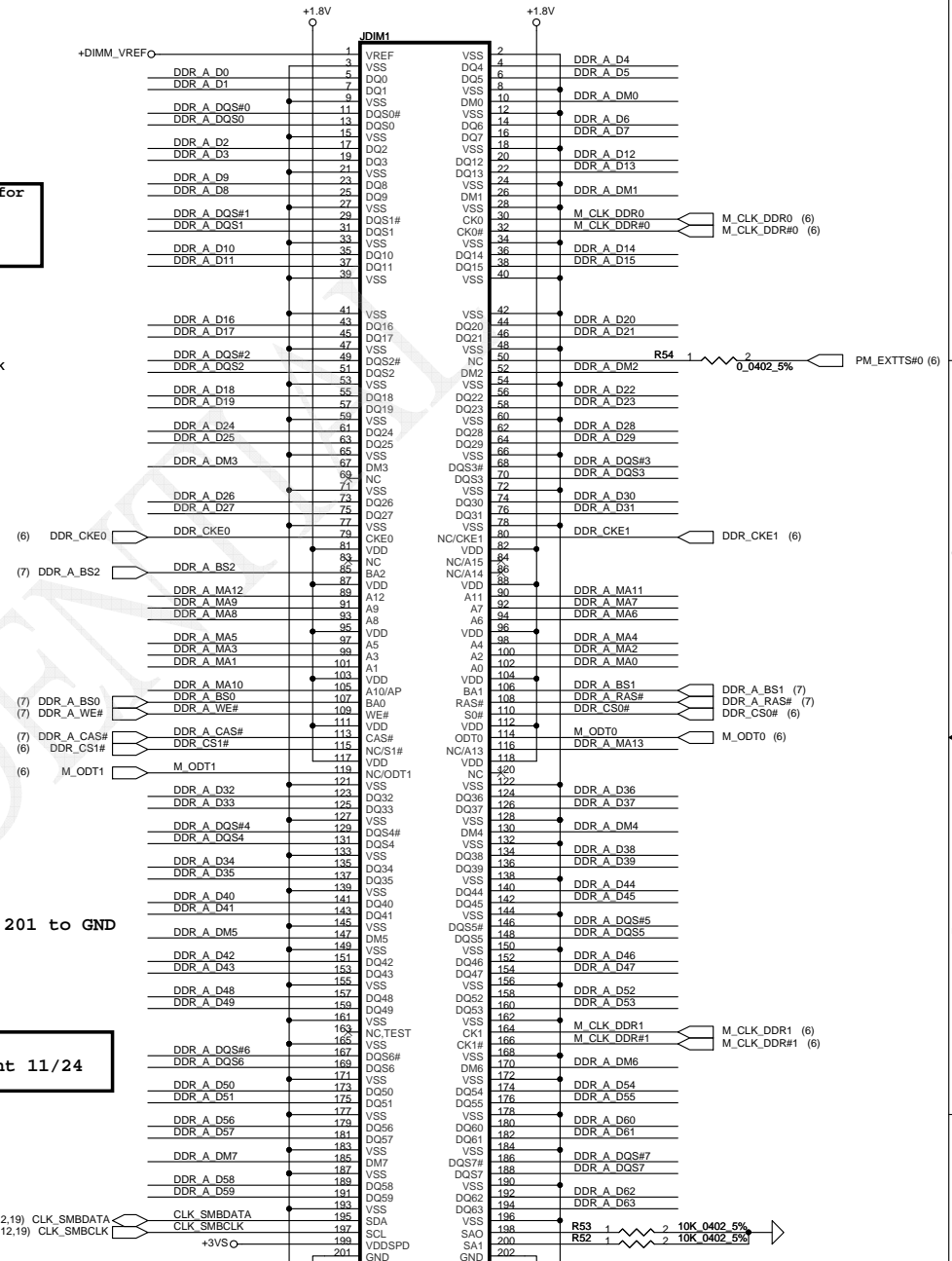
Layout Note:
Place these resistor
closely DIMMA, all
trace length
Max=1.3"

Share +DIMM_VREF for
1.DDRII VREF
2.GMCH SM_VREF_0
SM_VREF_1



For EMI DDR issue

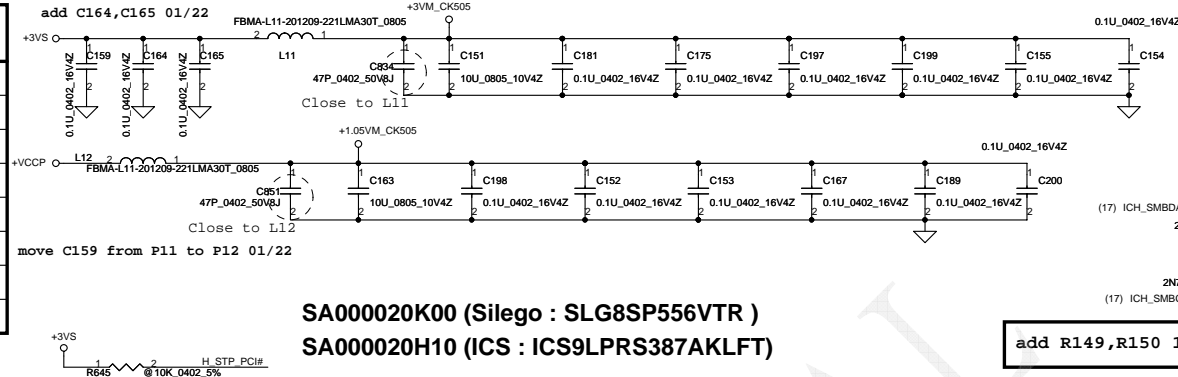
del C94 C95 01/22



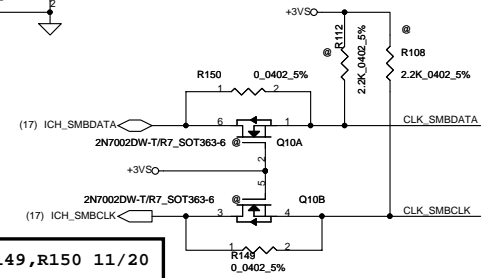
DIMMA

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



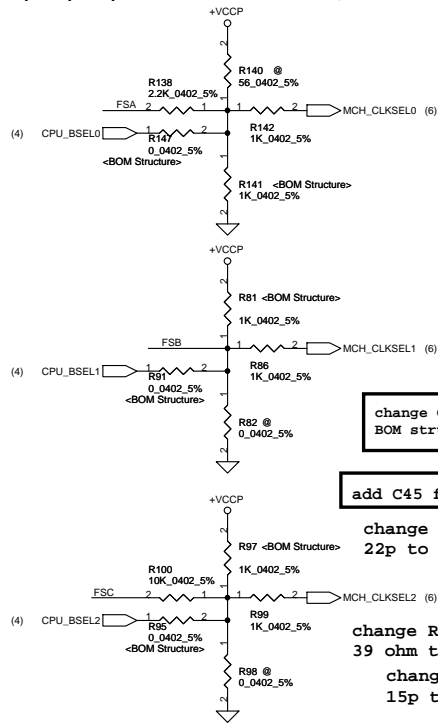
change R112,R108,Q10A,Q10B
BOM structure 11/20



```
add R149,R150 11/20
```

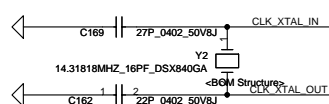
SA000020K00 (Silego : SLG8SP556VTR)
SA000020H10 (ICS : ICS9LPRS387AKLFT)

```
change R141,R140,R147,R81,R91
R82,R97,R95,R98 BOM structure 12/29
change R141,R140,R147,R81,R91
R82,R97,R95,R98 BOM structure 01/17
```



```
1 = Pin24/25 : SRC_0 / SRC_0#
    Pin28/29 : 27M/27M_SS
```

For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed



change C162 from 27P to 22P 01/23

del R143 and CLK_SD_48M 11/21

Change R137 from 12 ohm
to 33 ohm 11/21

change R137 BOM structure 12/15
add R143 12/15

del R143 12/15

change C32 from 10P to
15p ohm 02/06

change R137 from 33 to
39 ohm 02/06

change C32 C33 C42 C45
BOM structre 12/14

add C45 for keypart 12/14

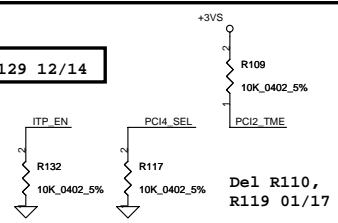
change C42,C45 from
22p to 15p 02/06

change R115,R121 from
39 ohm to 47 ohm 02/06

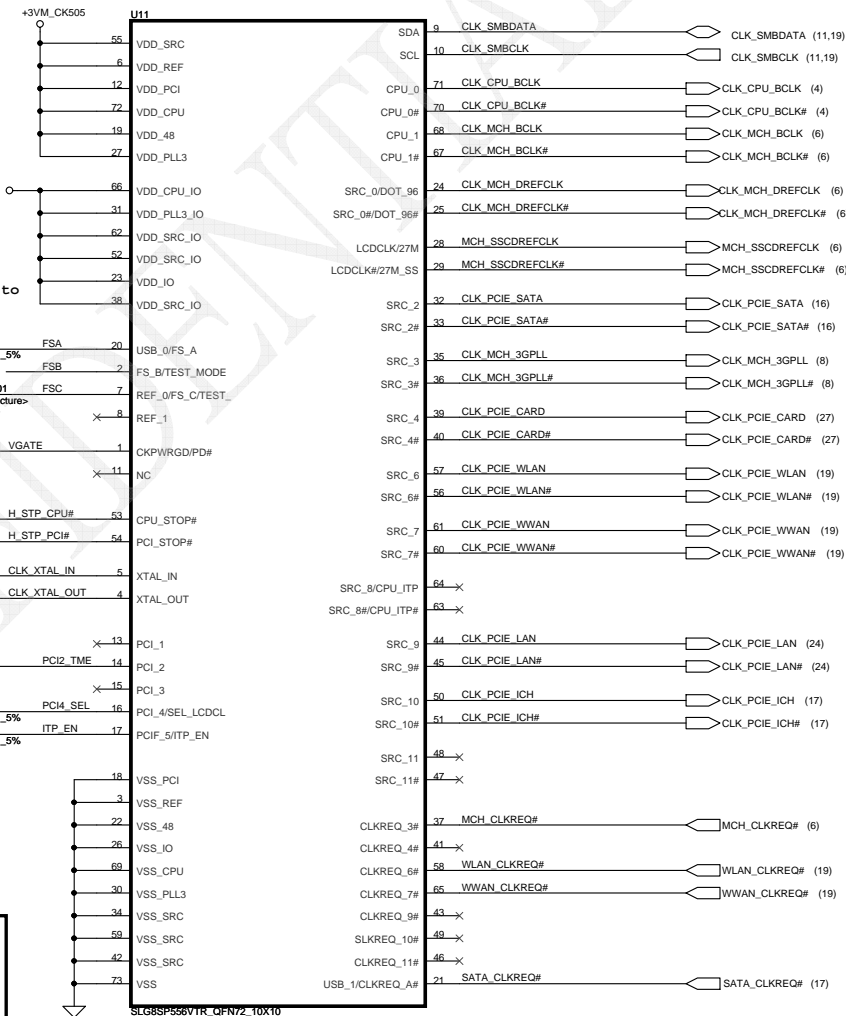
change c45 from
15p to 10p 02/24

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#

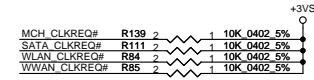


Del R110,
R119 01/17



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	SATA_HDD
SRC3	MCH_3GPLL
SRC4	PCIE_CARDREADER
SRC6	PCIE_WLAN
SRC7	PCIE_WWAN
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	

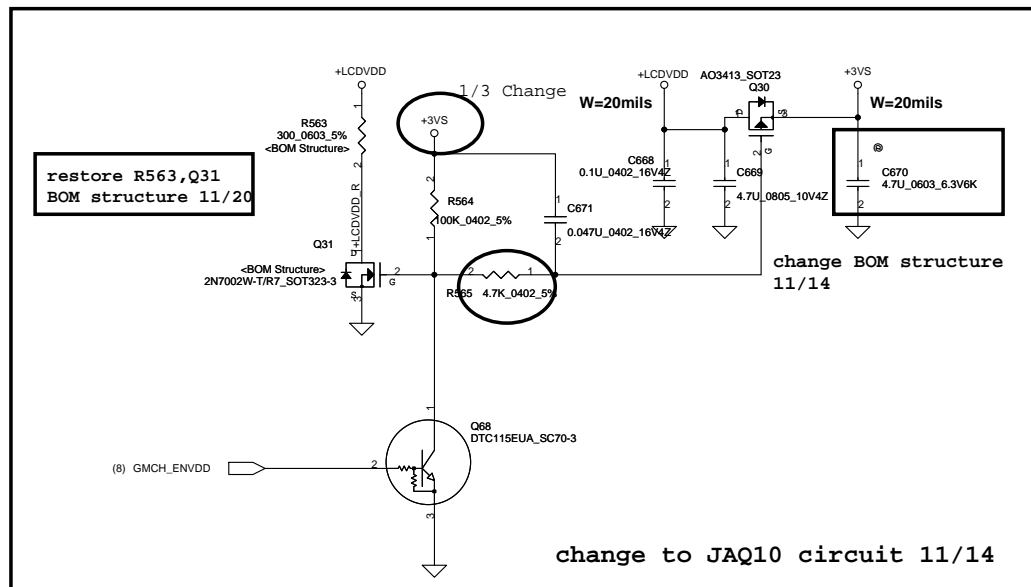


REQ PORT LIST

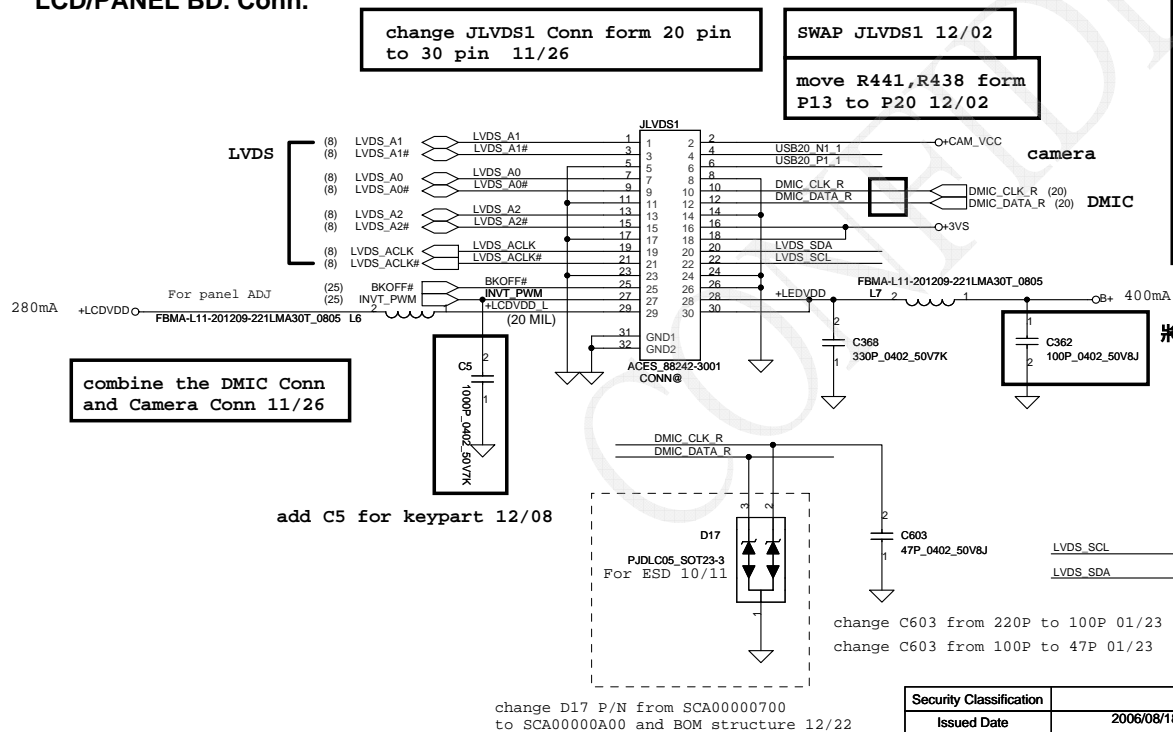
PORT	DEVICE
REQ_3#	MCH_3GPLL
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WWAN
REQ_9#	
REQ_10#	
REQ_11#	
REQ_A#	SATA

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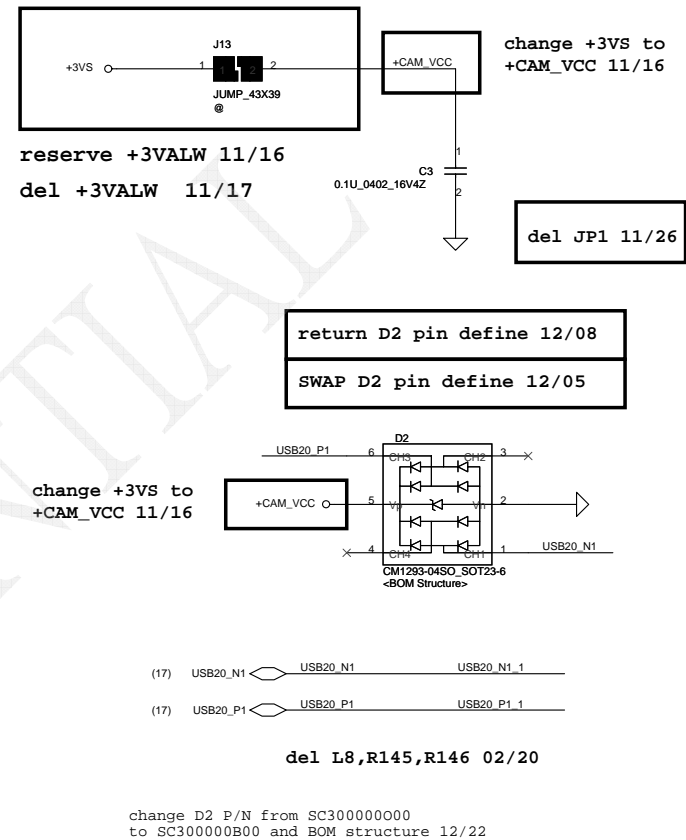
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



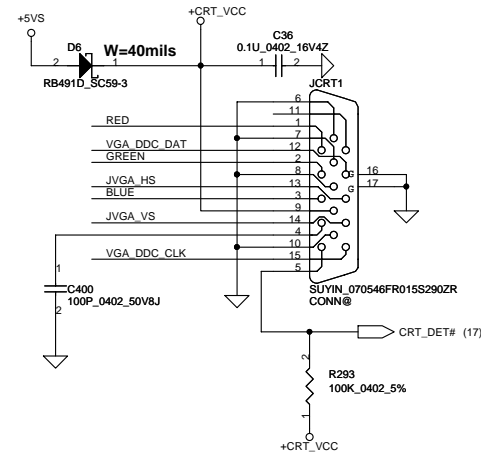
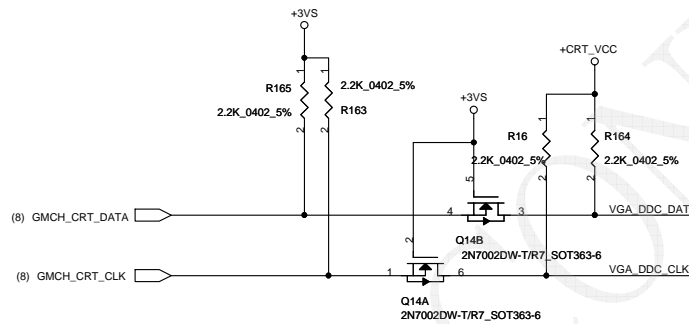
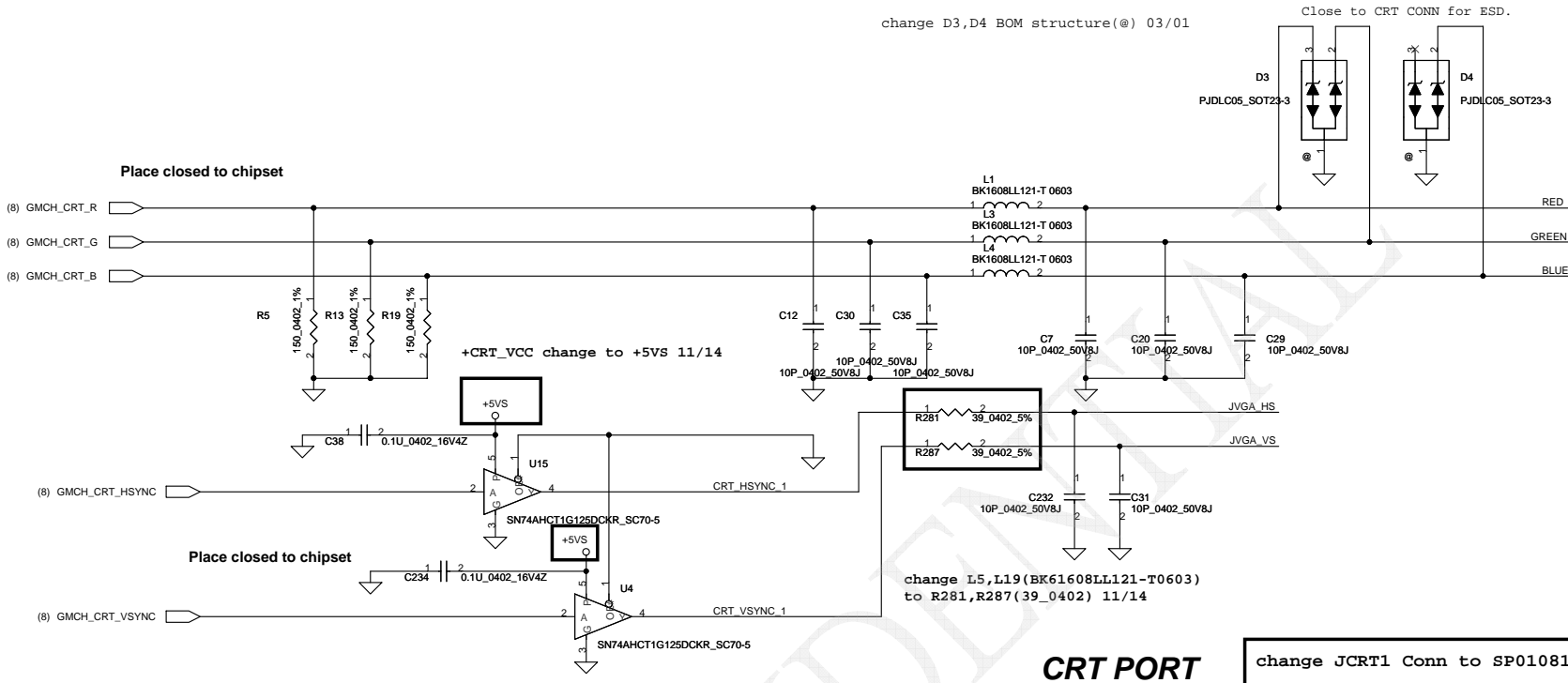
CMOS Camera CONN



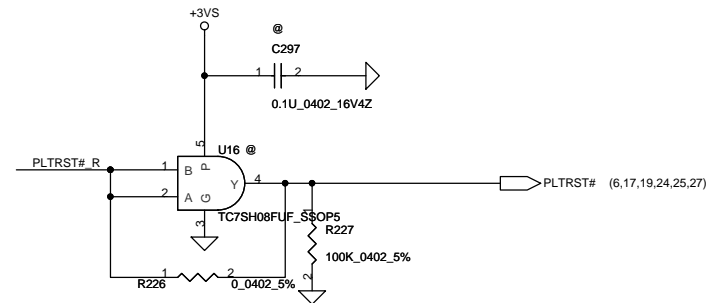
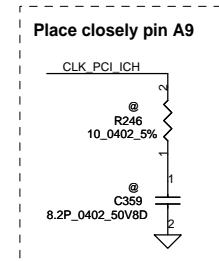
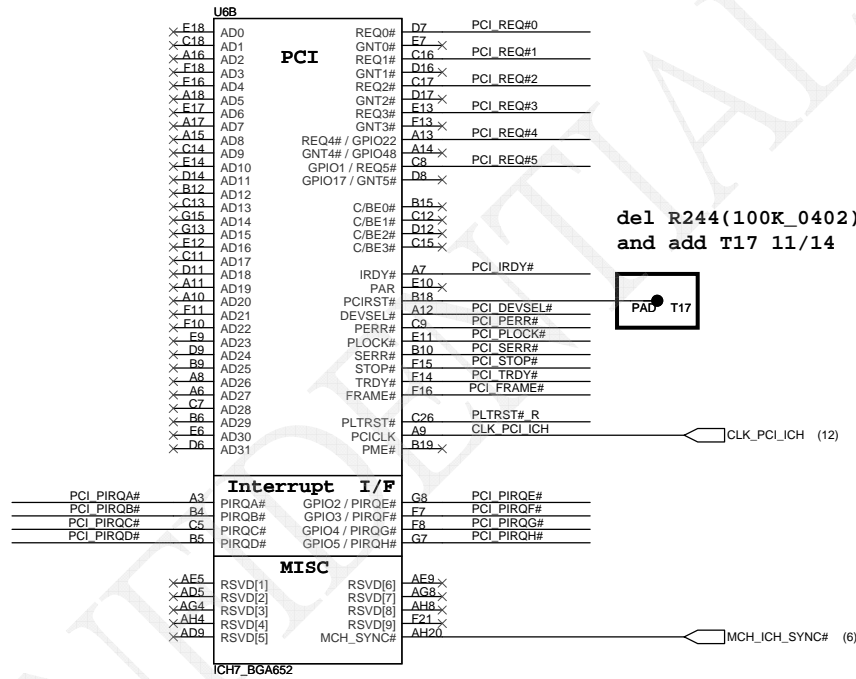
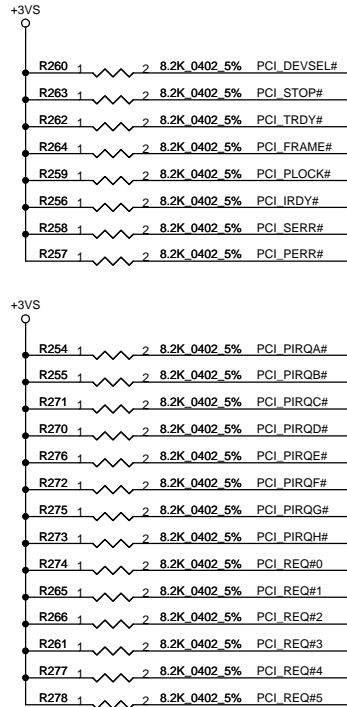
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change D3,D4 P/N from SCA00000G00
to SCA00000A00 and BOM structure 12/22

change D3,D4 BOM structure(@) 03/01

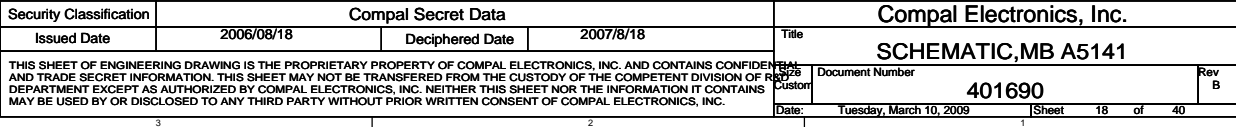


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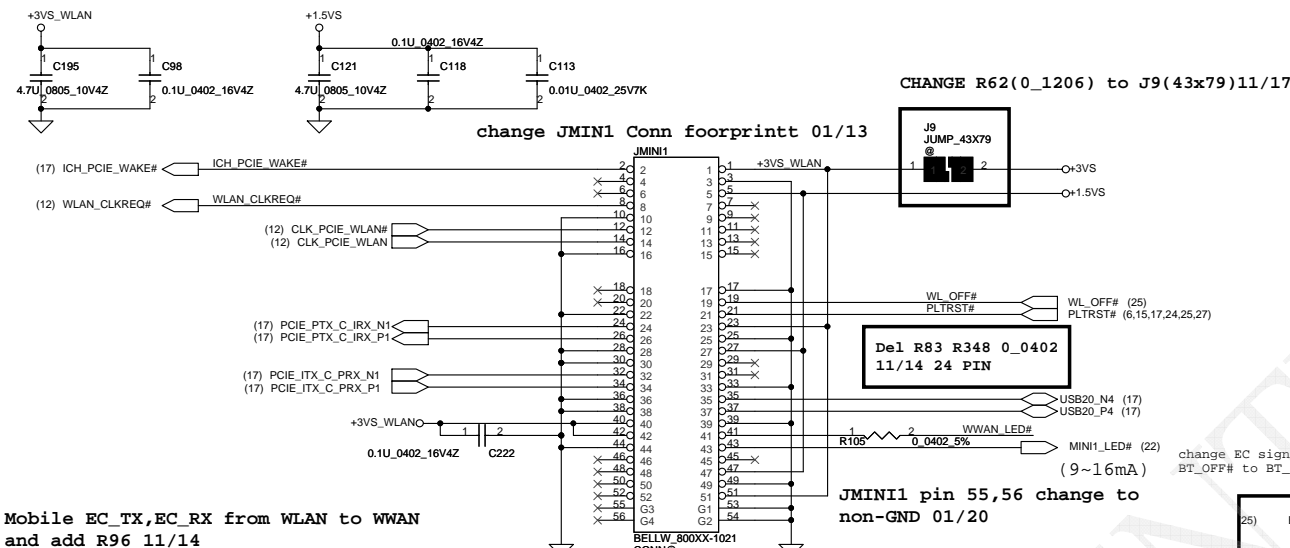


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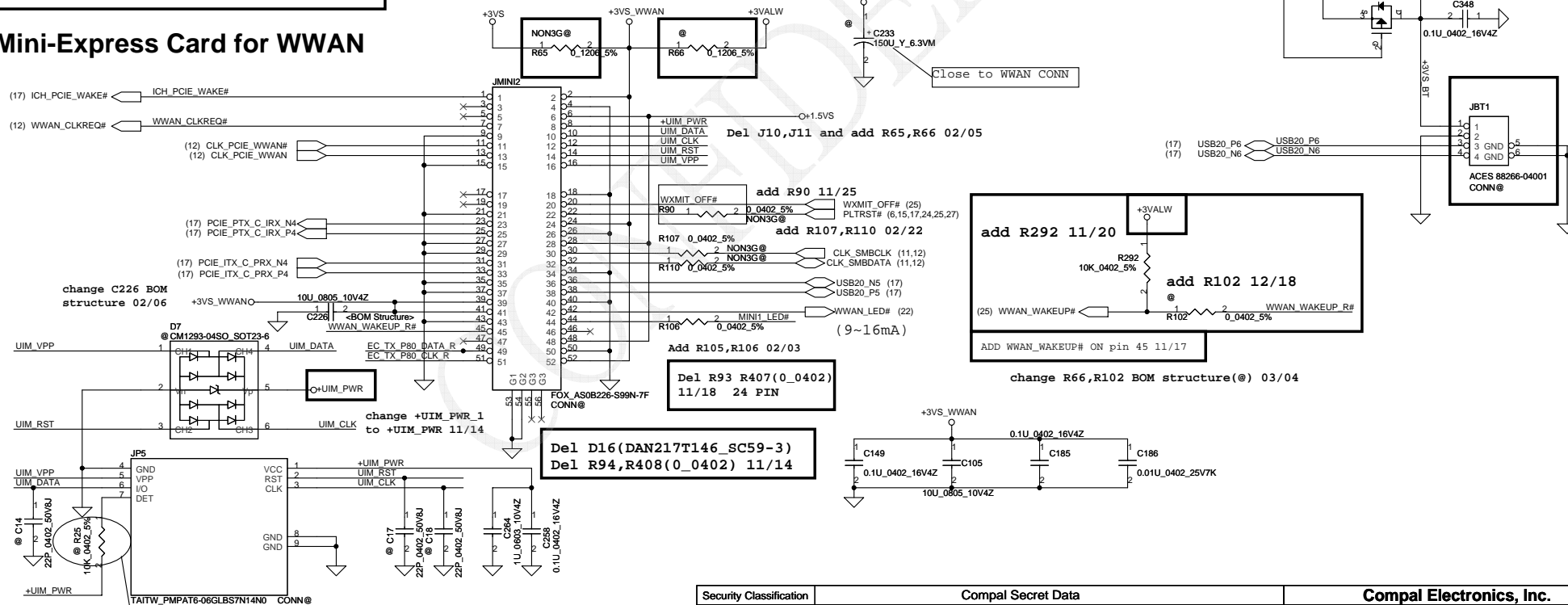
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Mini-Express Card for WLAN

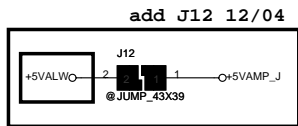


Mini-Express Card for WWAN

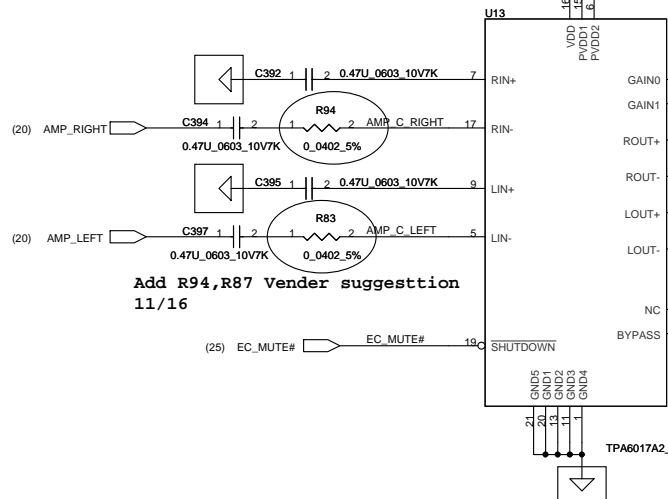


Reserve for SIM card does not meet rise time and pull-up is needed.

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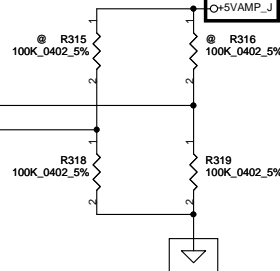


+5VS change to +5VALW 12/11



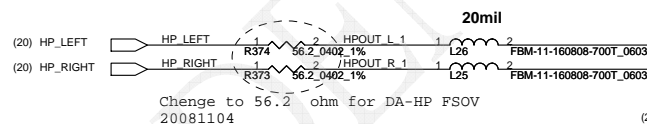
Add R94,R87 Vender suggestion 11/16

change +5VAMP to +5VS 12/02

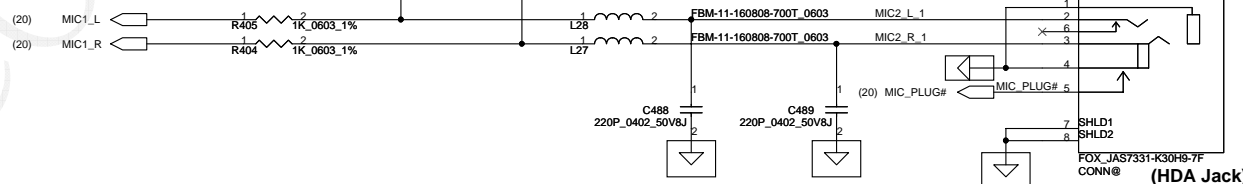
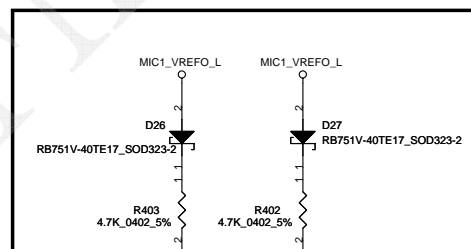


20081029 Update to 6dB

Analog ground change to digital ground 08/11/16

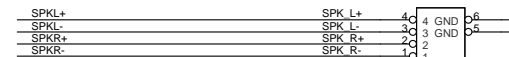


11/16



20mil

Int. Speaker Conn.



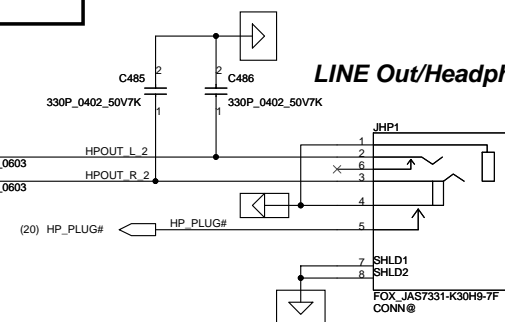
change JP20 Conn and pin design 11/26

del R388,R387,R386,R385,D10,D13 12/11

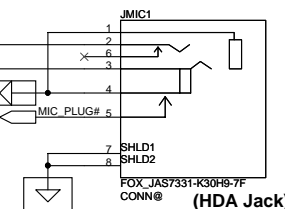
change JP20 Conn 01/16

SWAP JP20 01/20

LINE Out/Headphone Out



MIC JACK



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Move SATA HDD Conn to small board 11/21

SWAP JP7 pin define 12/03

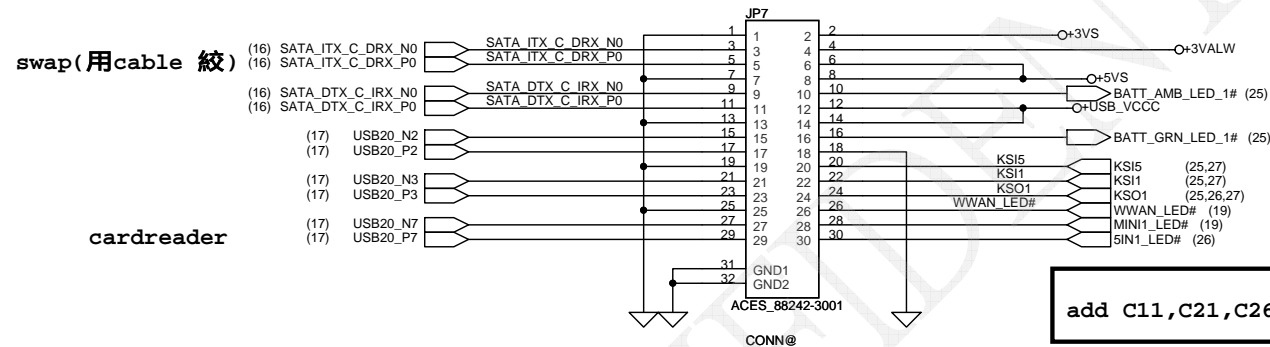
To cardreader/B Conn.

	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#

+3VS_READER change to +3VALW 12/15

add net name BATT_AMB_LED#
BATT_GRN_LED# 12/15

SATA&CARDREADER&USB Conn



add J15 J16 12/08

del J15,J16,C21 12/15

add C11,C21,C26,C27 for keypart 12/08

add C28 for keypart 01/14

del C11,C28,C26 01/21

del C26 02/03

ADD SATA&CARDREADER&USB Conn(JP7) 11/26

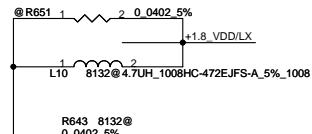
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Move Card Reader to small board 11/21

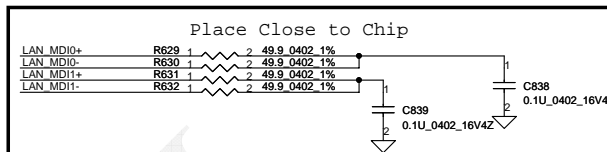
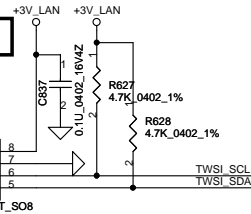
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change R644 from 0603 to 0805 12/31
change R643 from 0603 to 0402 12/31
change C841 from 0603 to 0402 12/31
add R651 0_0402 02/03
change C841 from 0402 1U to 0603 1U
02/03

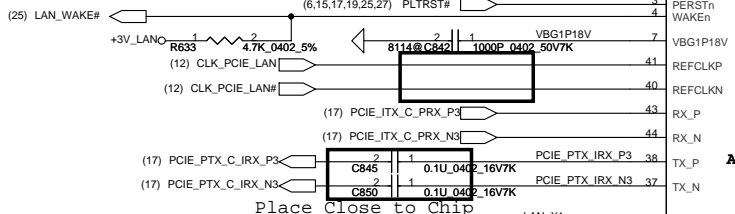


AR8114A: remove L1,C881,C885,R643, C841=1uF
AR8132:remove R644,R645, C841=0.1uF

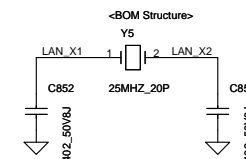
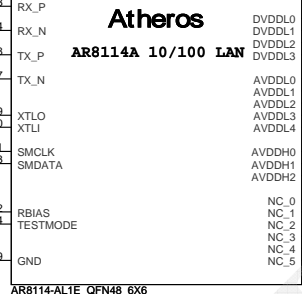


Chang C855 form 4.7U to 10U
11/16 vendor suggest

del C843,C844 12/02



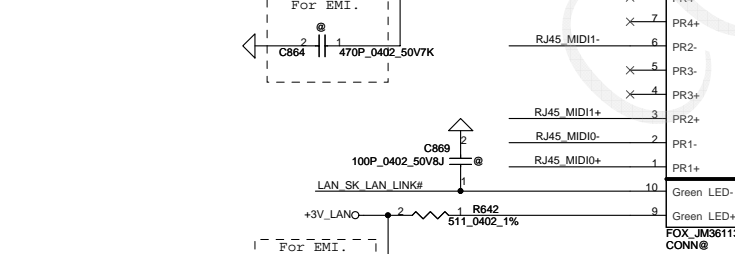
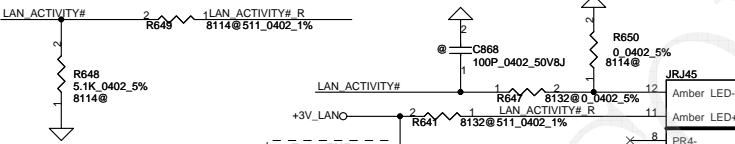
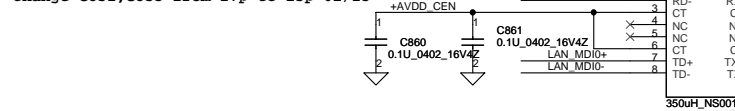
Atheros
AR8114A 10/100 LAN



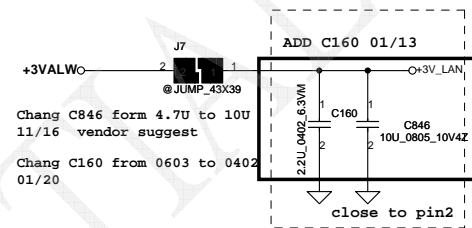
change C852,C853,Y5 BOM structure 12/15
add C55 on page 24 12/15

del C55 12/16

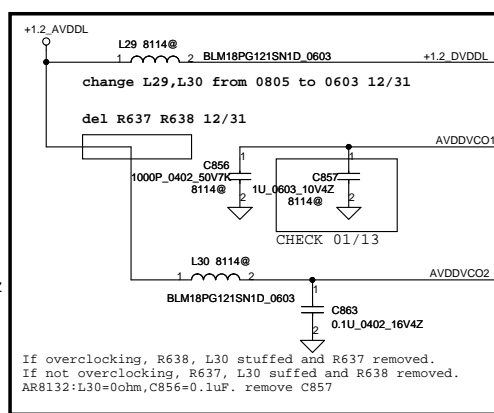
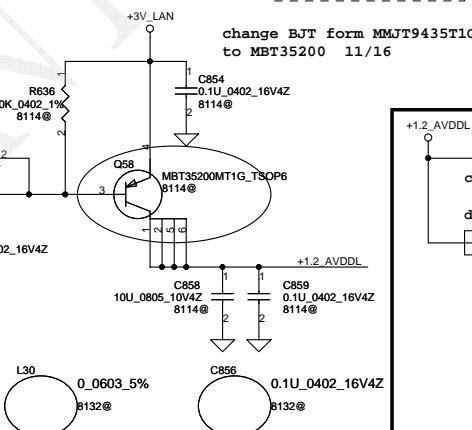
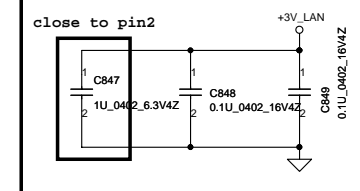
change C852,C853 from 27p to 15p 01/23



change JRJ45 Conn 11/26



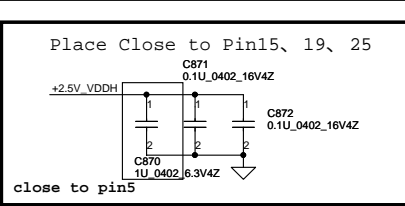
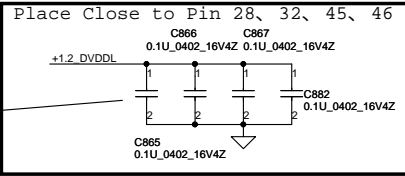
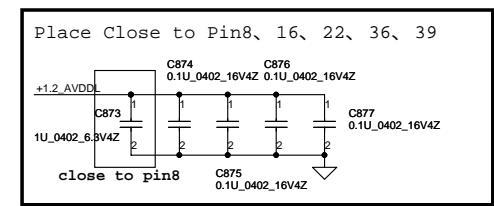
Layout Notice : Place as close
chip as possible.
change C847 from 0.1u to 1u 12/02



change L29,L30 from 0805 to 0603 12/31
del R637 R638 12/31

change L30,C856,C857 BOM structure 12/22

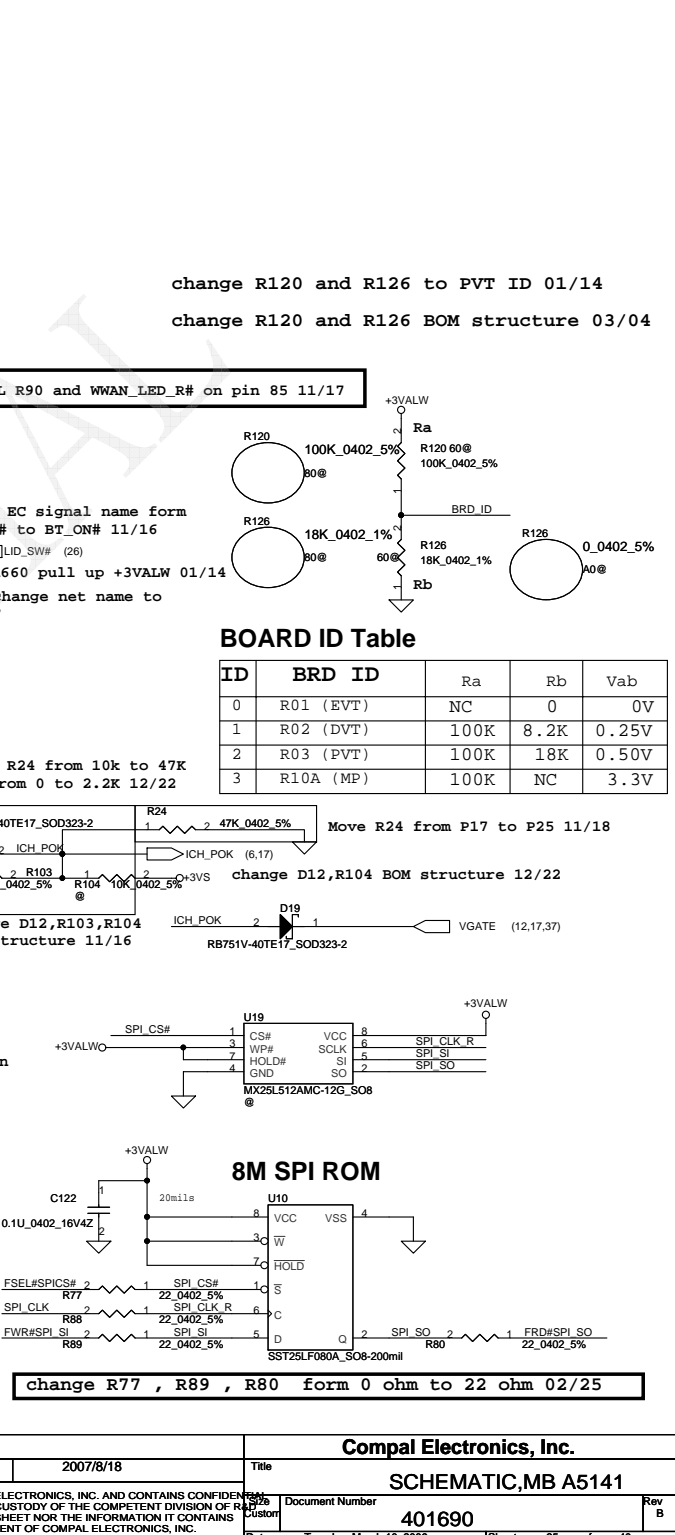
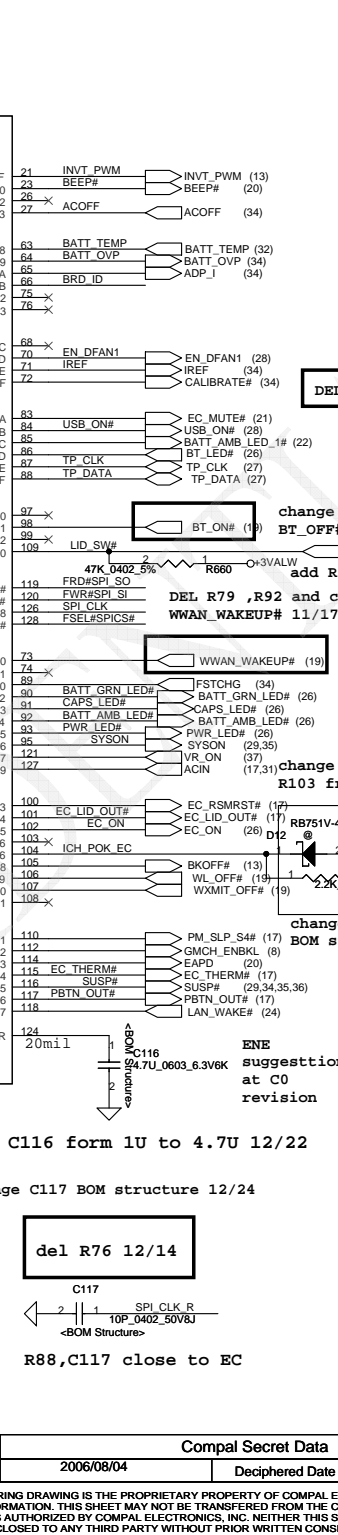
change C873 from 0.1u to 1u 12/02



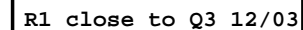
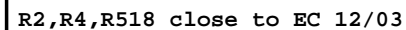
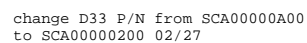
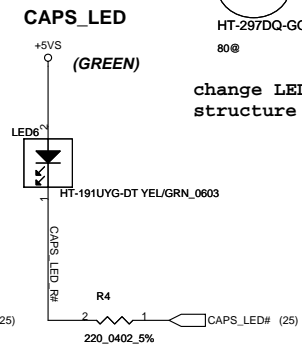
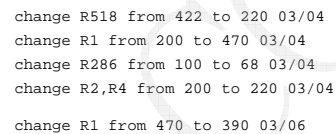
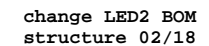
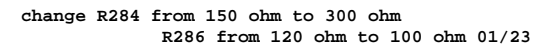
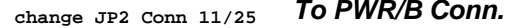
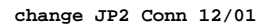
C865 close to Pin46
AR8114A: C865=0.1uF
AR8132:C865=1uF

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R125 ✓ ✓ ✓ 2.2K_0402_5%

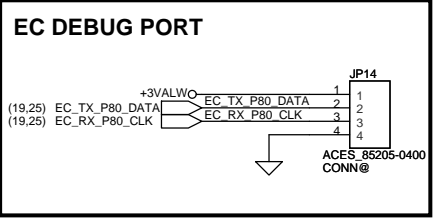
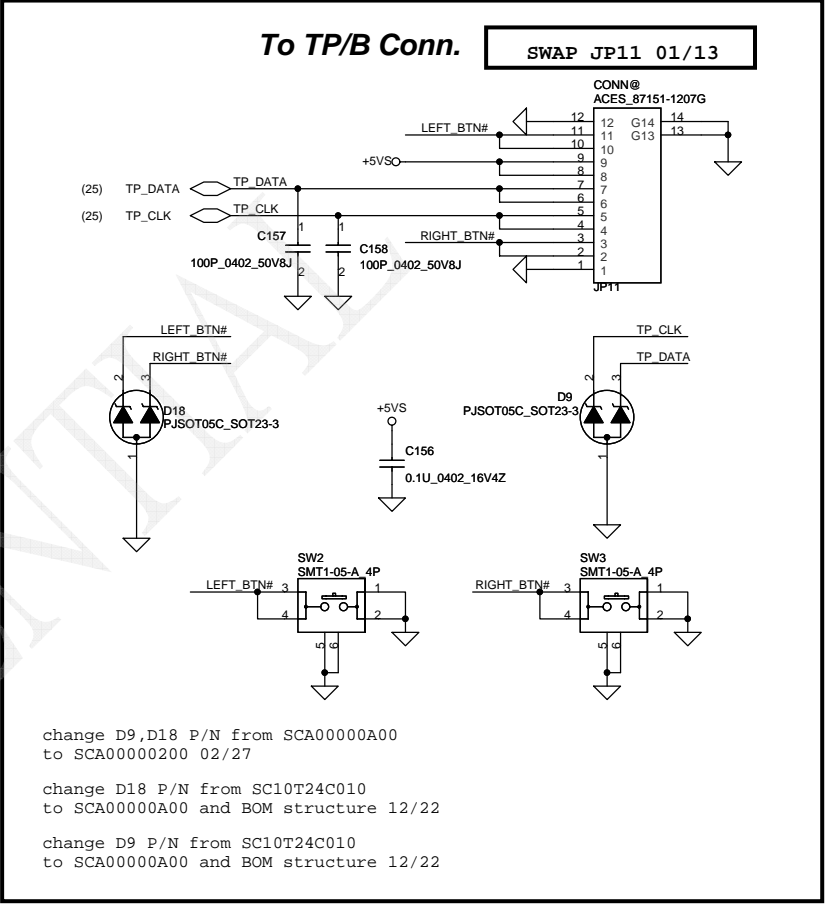
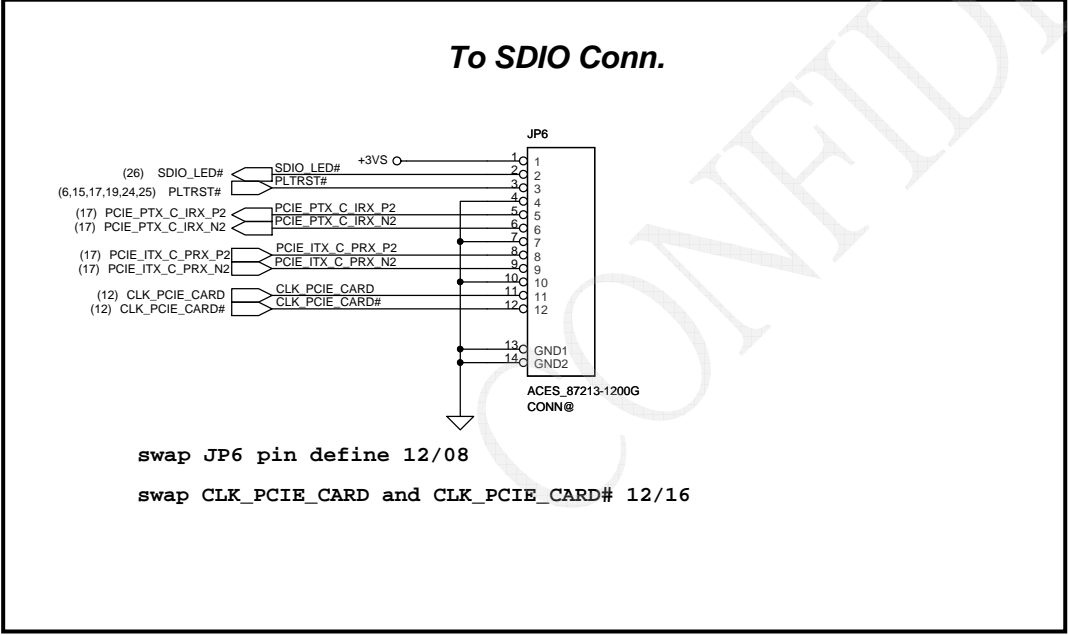
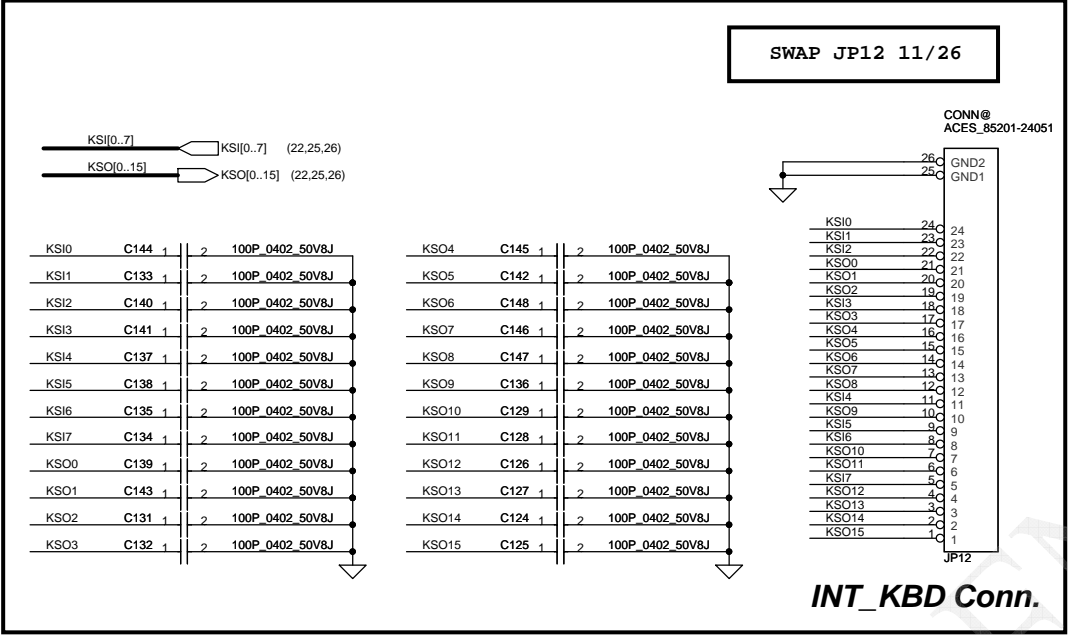


change J1,J3(43 x 79) to
R186,R193(0_0805) 11/16

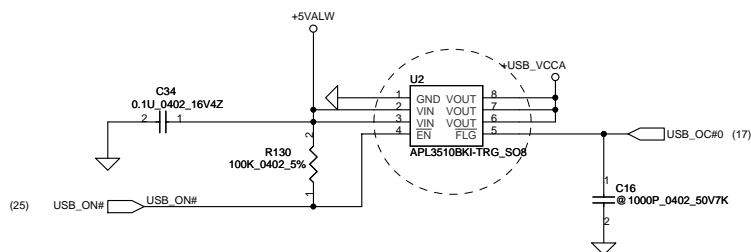


change R1,R2,R4 from 300 to 200 ohm 02/06

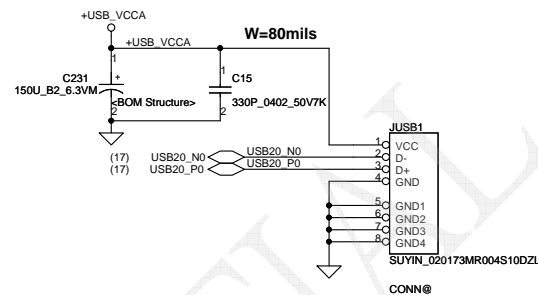
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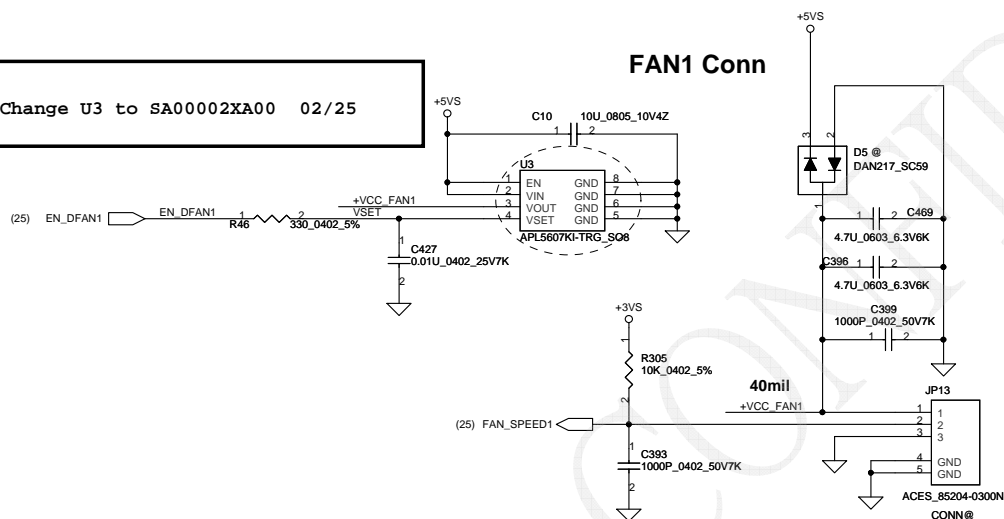
change U2 from SA000039E00 to SA000033H00 02/27



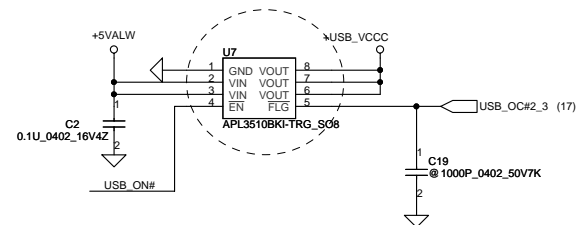
USB CONN. 1



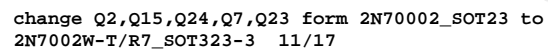
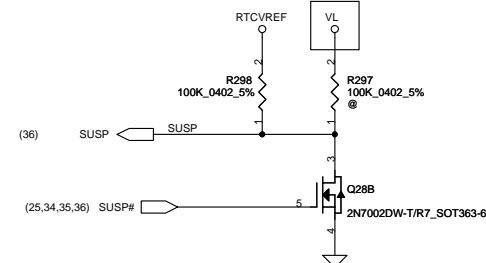
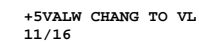
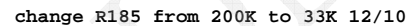
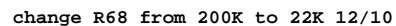
Change U3 to SA00002XA00 02/25



U7 Change to SA000039E00 02/25

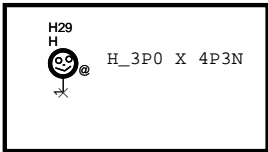


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change R18,R169,R280,R61,R279
Q2,Q15,Q24,Q7,Q7,Q23 BOM structure 11/16

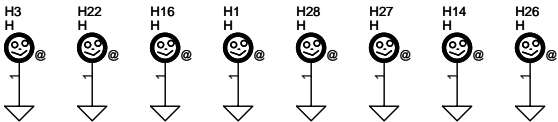
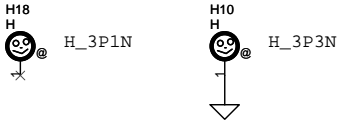
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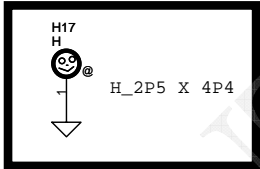
update Screw 12/04

del H11 H_3P0N 12/10

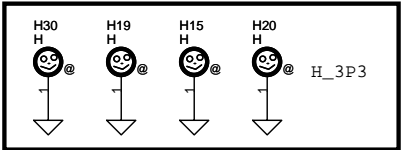
change H18 from 3P2N to 3P1N 02/22



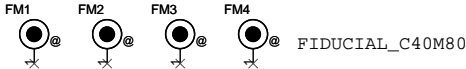
del H31 01/16



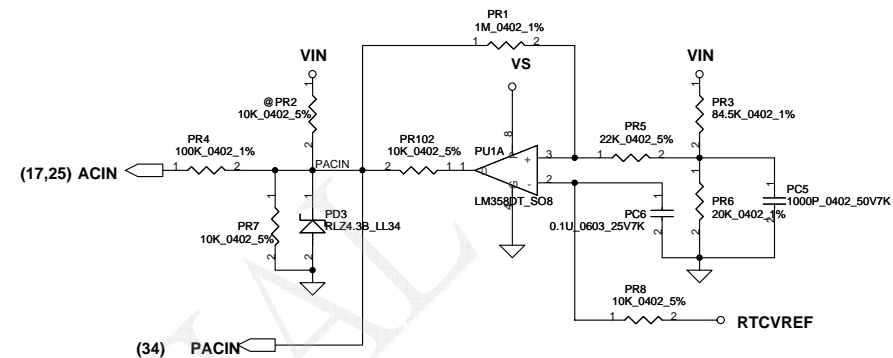
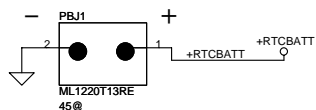
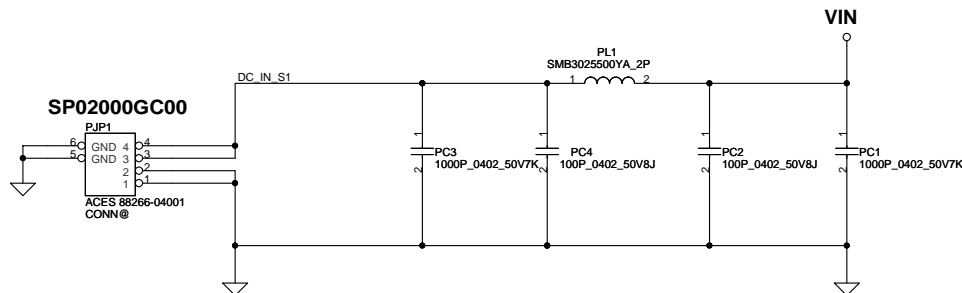
change H17 from H_2P5 to H_2P5 X 4P4



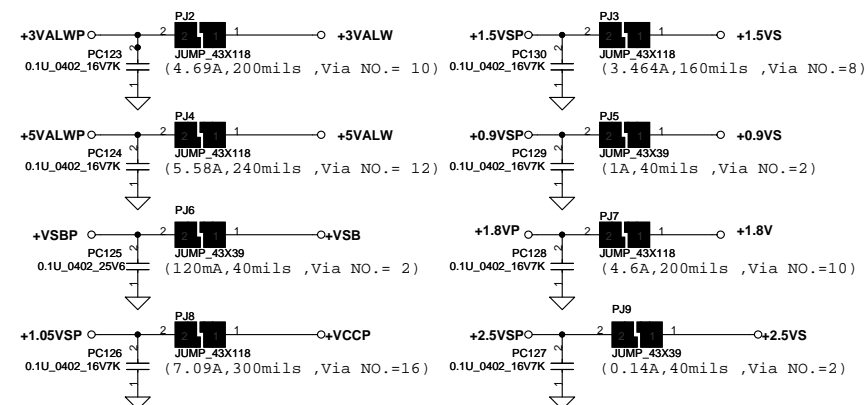
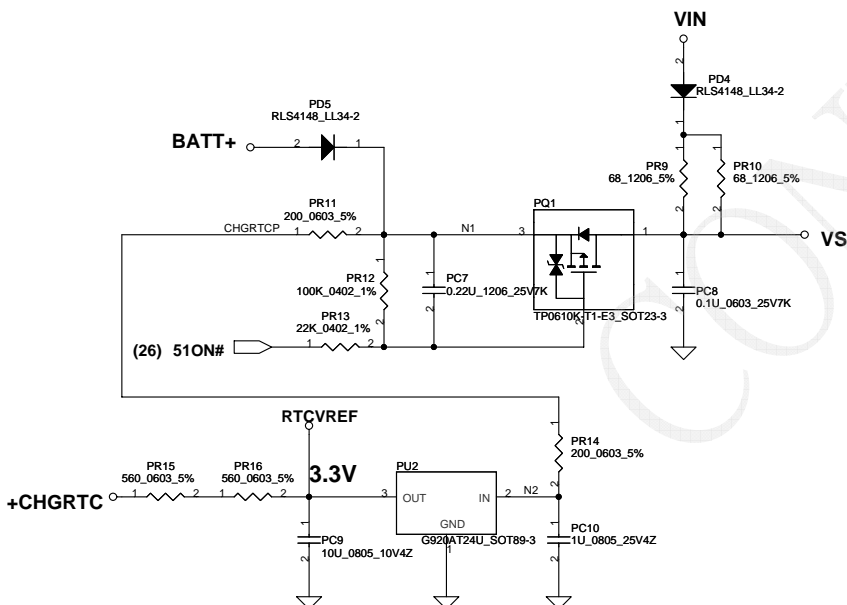
add H32 12/17
modify H15,H19,H20,H29,H30 12/17
update H15,H19,H20,H30 from 3P8 to 3P6 01/22
update H15,H19,H20,H30 from 3P6 to 3P3 02/22



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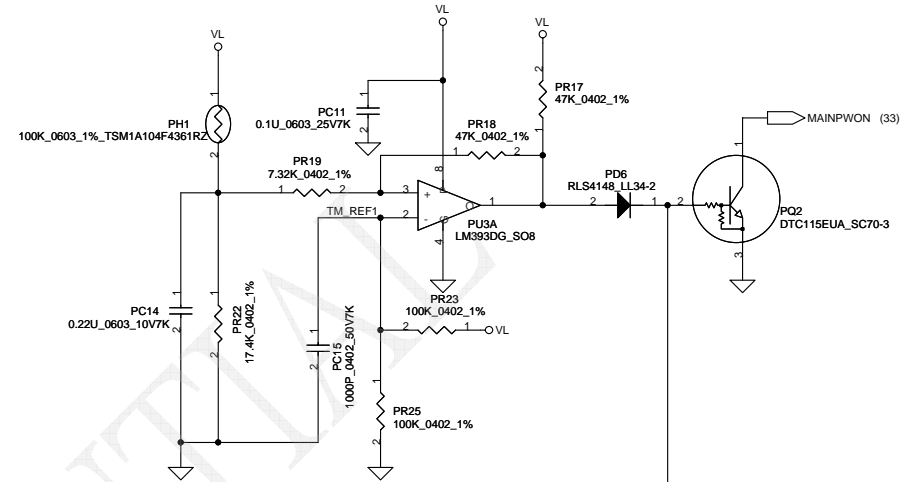
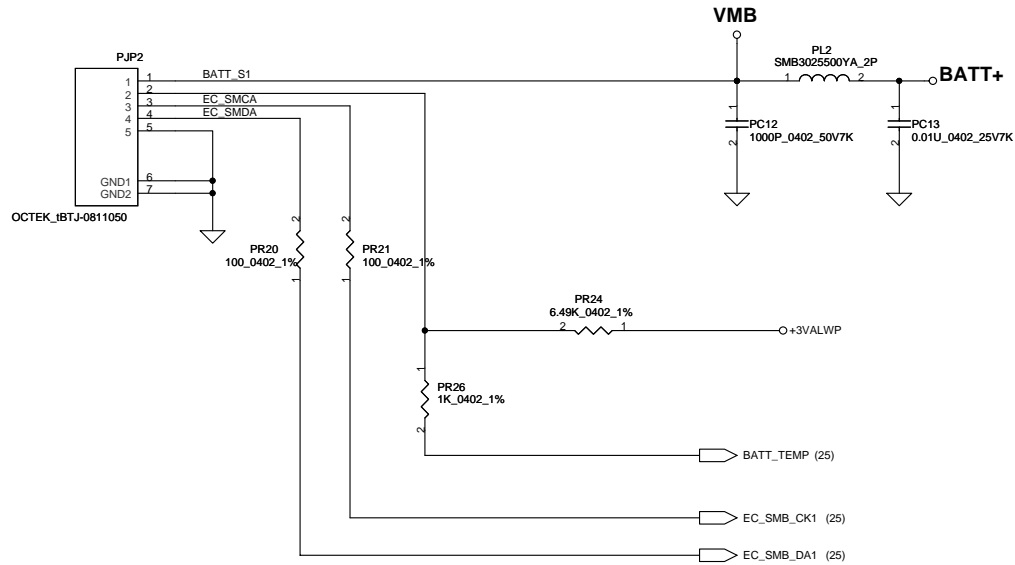


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

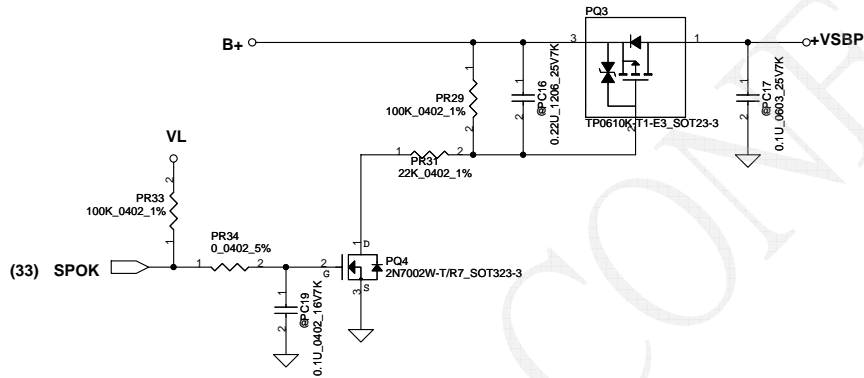
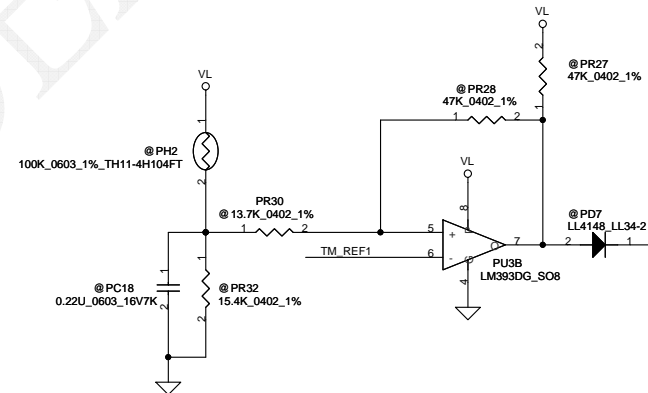


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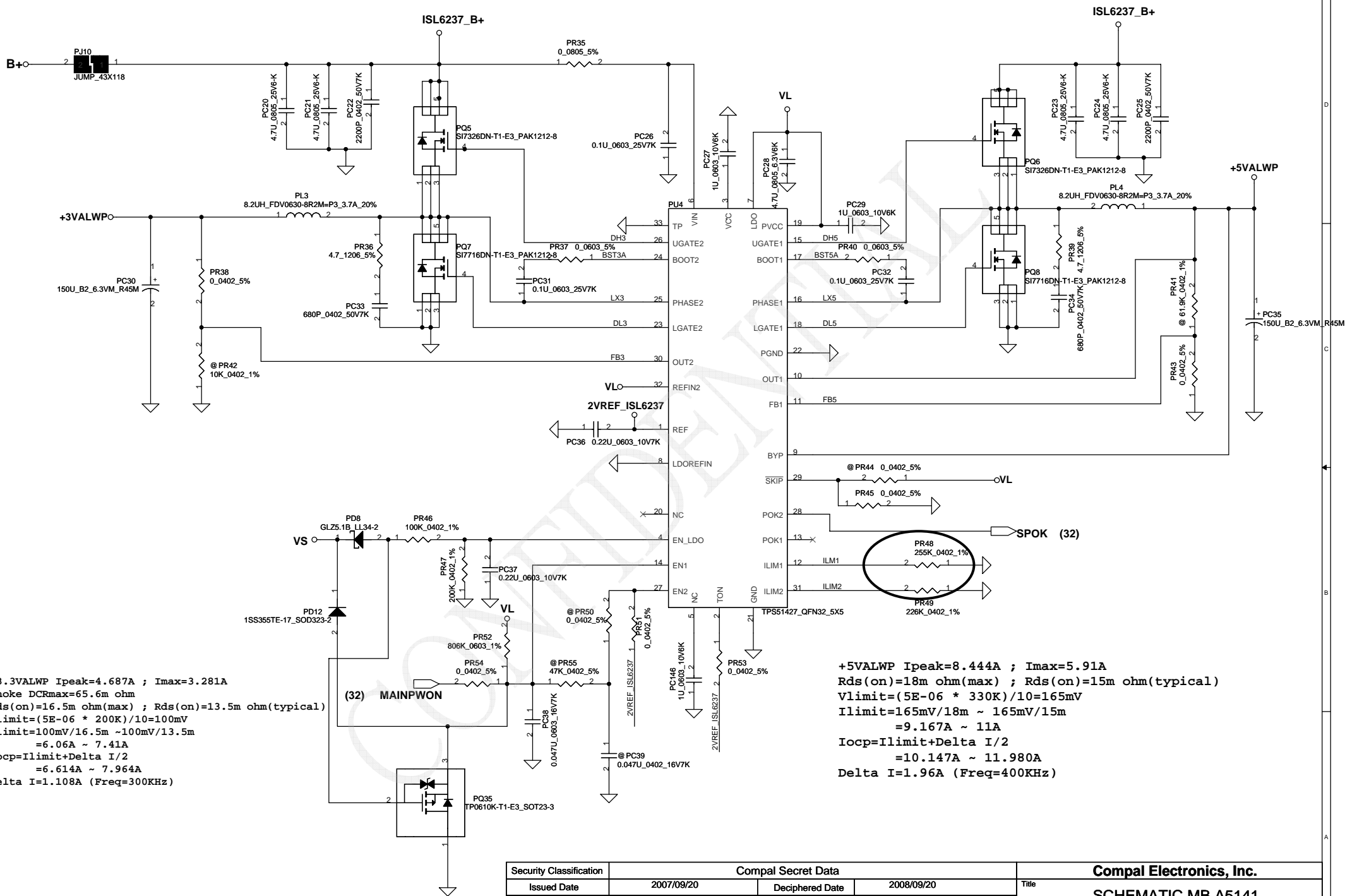
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



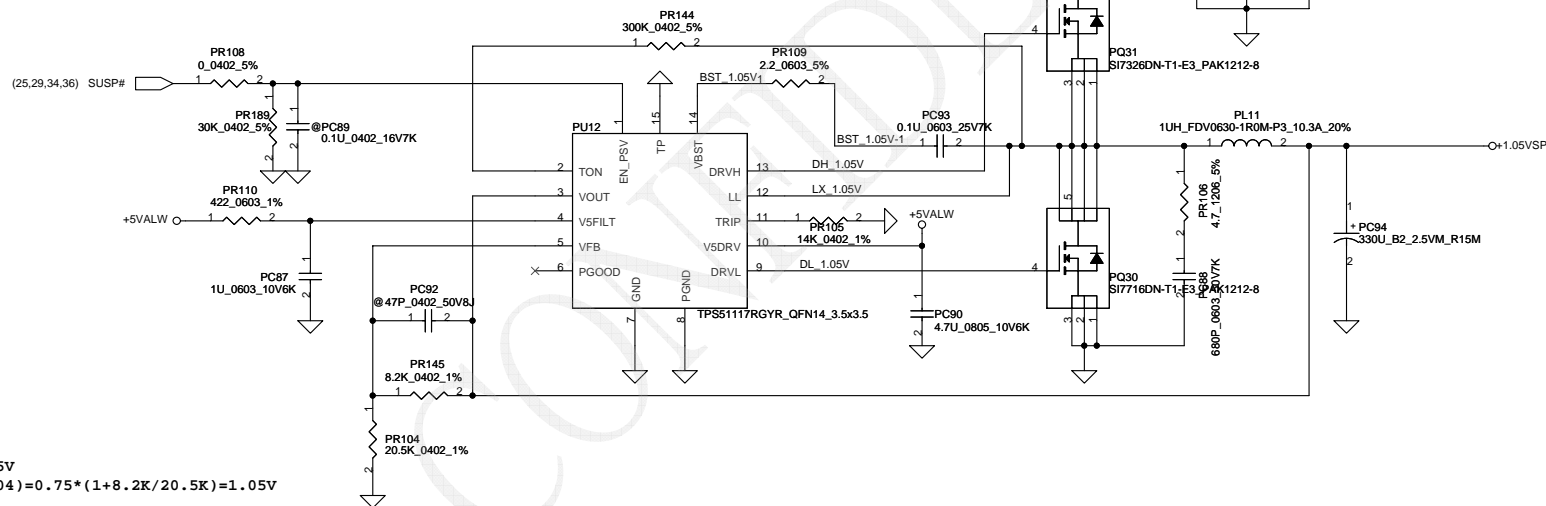
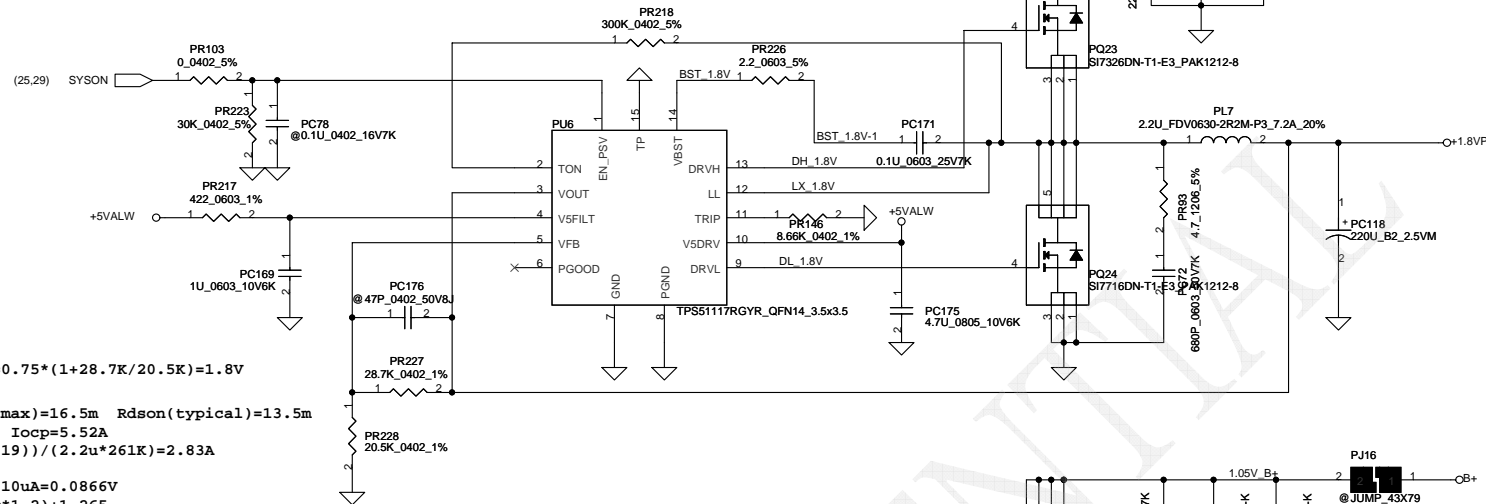
PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



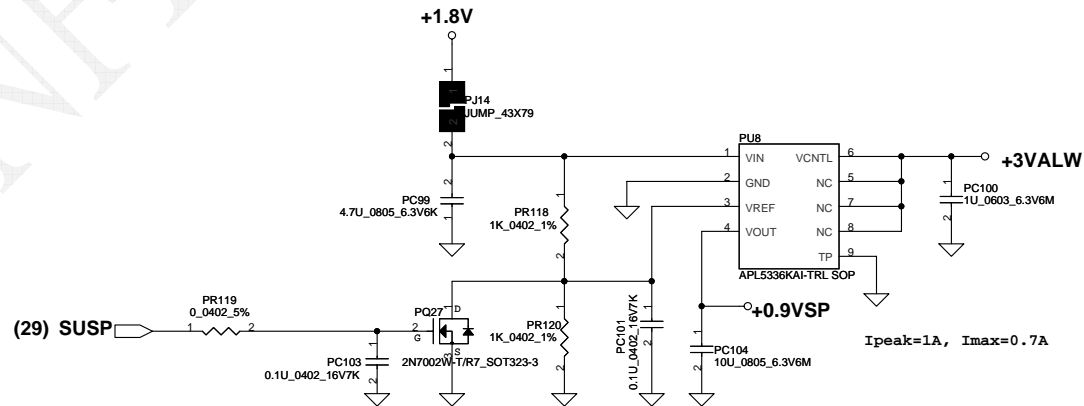
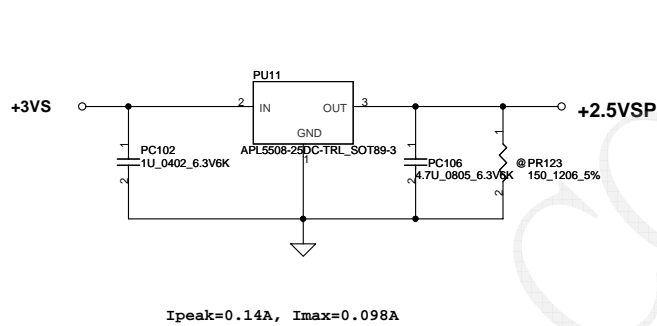
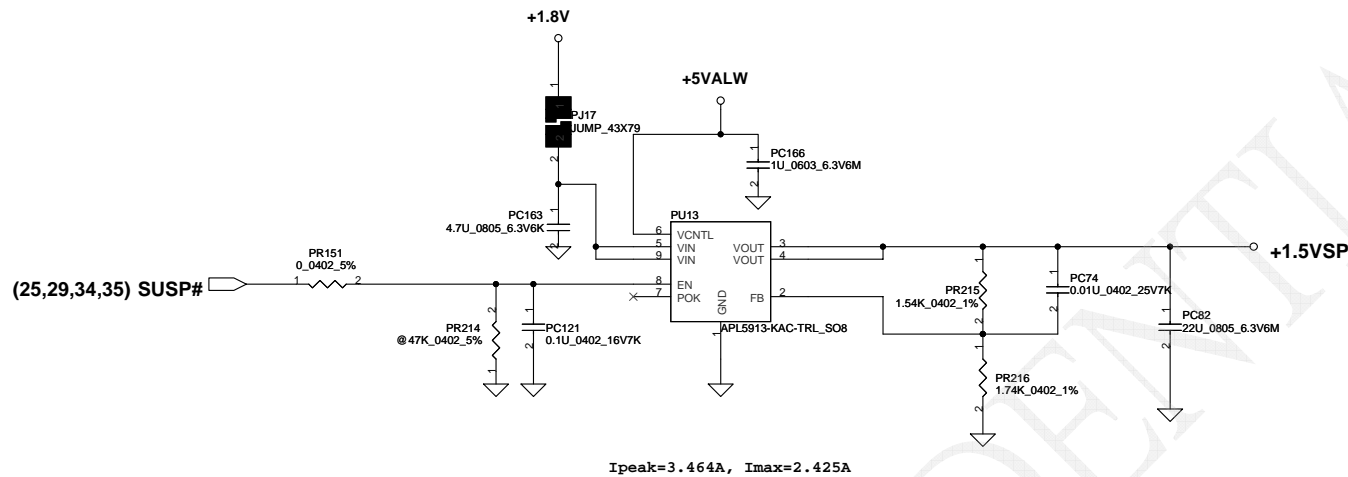
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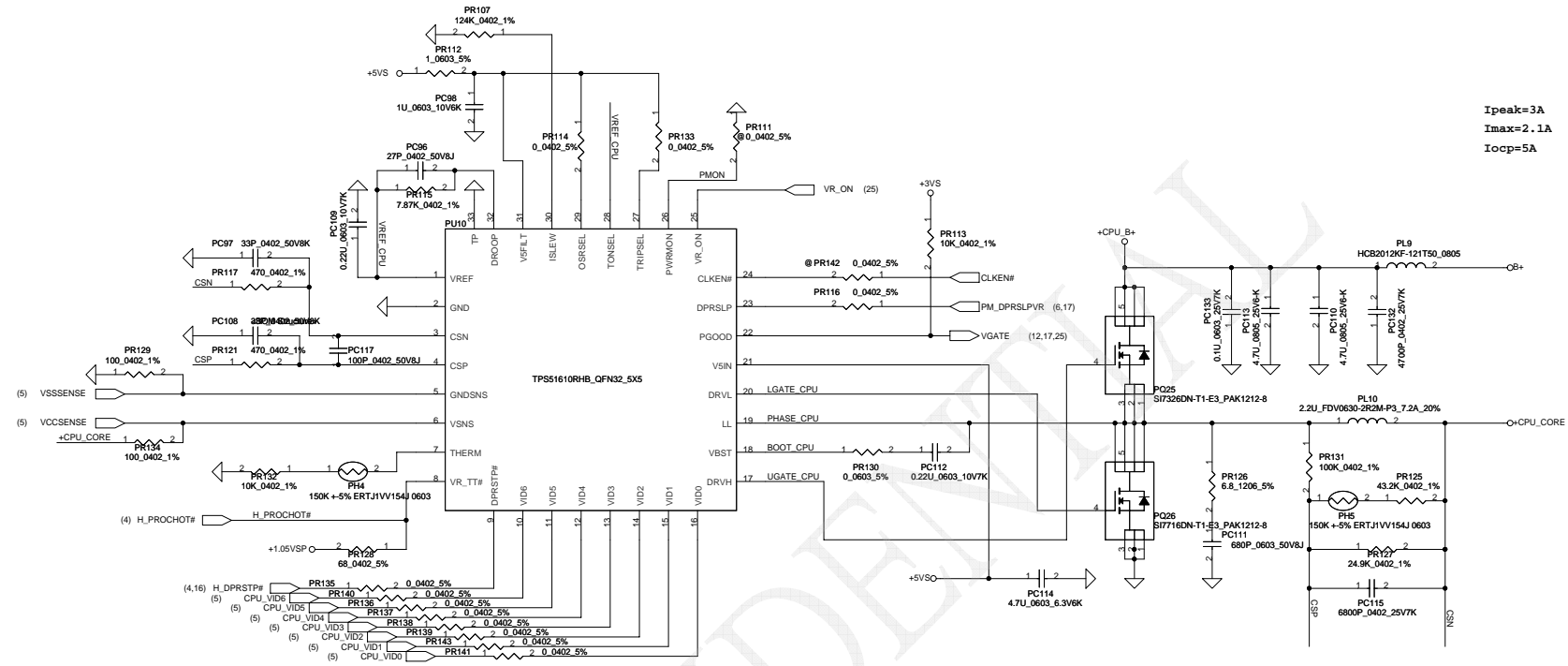
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Ipeak=3A
Imax=2.1A
Iocp=5A

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify CPU OTP circuit	For thermal team request	0.1	31	Cahnge PR19 to SD034732180 (S RES 1/16W 7.32K +-1% 0402) Cahnge PR22 to SD034174280 (S RES 1/16W 17.4K +-1% 0402)	09/01/14	DVT
2	Modify 3/5V output cap	design change	0.1	32	Cahnge PC30 to SGA00004H00 (S POLY C 150U 6.3V M B2 LESR25M PSL H1.9) Cahnge PC35 to SGA00004H00 (S POLY C 150U 6.3V M B2 LESR25M PSL H1.9)	09/01/14	DVT
3	Modify Charger modify	redulate charger ADJ voltage	0.1	33	add PR211 to SD034301380 (S RES 1/16W 301K +-1% 0402) add PR220 to SD034499380 (S RES 1/16W 499K +-1% 0402)	09/01/14	DVT
4	Modify 1.8v/1.05v boost circuit	for APW7141 issue	0.1	34	Cahnge PR226 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603) Cahnge PR109 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	09/01/14	DVT
5	add all sunbber	for 3G and EMI team request	0.1	34	add all sunbber	09/01/14	DVT
6	Modify HMOS and LMOS	for cost down	0.1	34	H-side to SB000001A00 (S TR SI S412DN-T1-GE3 1N POWERPAK1212-8) L-side to SB000001400 (S TR IRFH3707TRPBF 1N PQFN)	09/01/14	DVT
7	add input capacitance	for 3G solution	0.1	34	add PC41 PC46 SE074222K80 (S CER CAP 2200P 50V K X7R 0402)	09/01/21	DVT
8	modify 1.05v TRIP R	modify ocp point	0.1	34	modify PR105 to SD034140280 (S RES 1/16W 14K +-1% 0402)	09/02/02	DVT
9	modify 3V/5V OCP point	design change	0.1	34	Cahnge PR48 SD034255380 (S RES 1/16W 255K +-1% 0402)	09/02/02	DVT
10	modify 3V/5V OCP point	design change	0.1	34	Cahnge PR49 SD034226380 (S RES 1/16W 226K +-1% 0402)	09/02/18	PVT
11	modify chager circuit	design change	0.1	34	Add PQ44 SB000006800 S TR 2N7002W T/R7 1N SOT-323	09/02/18	PVT
12	modify chager circuit	design change	0.1	34	Add PQ34 SB301150000 S TR DTC115EUA NPN (UMT3)	09/02/18	PVT
13	modify chager circuit	design change	0.1	34	Add PR152 SD034470280 S RES 1/16W 47K +-1% 0402	09/02/18	PVT
14	modify chager circuit	design change	0.1	34	Add PQ33 SB101440200 S TR DTA144EUA PNP UMT3	09/02/18	PVT
15							
16							
17							
18							
19							
20							
21							
22							
23							

KAV10

A-TEST Change

- <8/25>
1. Update Power SCH
<8/26>
1. Update Power SCH
2. Change
 D7 SC300000D00 to SC300000000
3.Change
 C49、C50 SE071180K80 to SE071180J80
<8/27>
1. Updata Power SCH
2. Modify
 RJ45 temp footprint FOX_JM3611A-R4122-7F_12P-T
<8/28>
1. Updata Power SCH
<9/1>
1. Updata Screw
<9/5>
1. SWAP USB20_1 Signal.
<9/10>
1. Remove Mini card pin55、pin56 的GND.
2. Change JREAD1.42、H26 to GNDA.
<9/12>
1. Swap 3G ESD pin neme.
<9/15>
1. Update Audio Jack footprint
2. Chngce R641、R642 300ohm to 511ohm for Arthros.
3. Update L footprint.
<9/16>
1. Update POWER SCH.
<9/17>
1. Update POWER SCH.
2. ADD R380、R383 for ESD.
<9/18>
1. Update ATHEROS 10/100 LAN <AR8132/AR8114>
<9/24>
1. Change C870 0.1u to 1u.
<9/26>
1. R88 change to 0ohm.

B-TEST Change

- <10/21>
1.Remove C389 for Audio can't detect issue on page 16
2.Add KSO1/KSO2 PU +3VALW on page25
3.Add R205 for schematic mistake on page 04
4.Change EC RST to FLTRST on page 25
5.Add J8 to cost down Audio LDO on page 20
6.Add R72 to reserve +3VALW for 3G on page 19
7.Reserve C238 for CRTDAC on page 10
8.Add R87 for Debug card on page 19
9.Change C108/C255 to 0.1uF for random hang issue
10.Change JP3 pin assignment on page 28
<10/21>
1. Update Power SCH
<10/29>
1. Audio AMP 10dB update to 6dB
<11/3>
1. Update Power SCH
<11/4>
1. Change R373、R374 to 56.2 ohm for DA-HP FSOV
2. Add C834、C851 for 3G noise
3. Change KB926 C1 to D2
4. Card reader RT5158E change to RT5159-GR
<11/5>
1. Swap D7 pin define
<11/10>
1. EC add R79、R90、R92 for SMS wakeup.

KAV60

A-TEST Change

- <2008/11/14>
1. change R28,R32 BOM structure on page 4
2. change LCD POWER CIRCUIT form KAW10 to JAQ10 on page 13
3. change C670 BOM structure on page 13
4. change L5,L19(BK61608LL121-T0603) to R281,R287(39_0402) on page 14
5. change +CRT_VCC to +5VS on page 14
6. del R244(100K_0402) and add T17 on page 15
7. change J6 jump size form 43 x 118 to shortpads on page 16
8. change R204 BOM structure on page 16
9. change Q11 from SOT23 to SOT323-3 on page 17
10.change USB OC# circuit on page 17
11.Del R186(0_0805_5%) and +1.5VS DMIPLLR on page 18
12.CHANGE R62(0_1206) to J9(43x39) on page 19
13.Del R83 R348 0_0402 on page 19
14.Mobile EC_TX,EC_RX from WLAN to WWAN and add R96 on page 19
15.CHANGE R65,R70(0_1206) to J10,J11(43x39) on page 19
16.change +UIM_PWR_1 to +UIM_PWR on page 19
17.Del D16(DAN217T146_SC59-3),R94,R408(0_0402) on page 19
18.change +5VS to +3VS on page 19
19.change EC signal name form BT_OFF# to BT_ON# on page 19
20.del Q21 on page 19
21.ADD PMOS SOFT START on page 19

- <2008/11/16>
1. +VDDA CHANGE TO +5VS on page 20
2. Analog ground change to digital ground on page 20
3. Del L22 on page 20
4. DEL R383 R382 R384 GNDA & GND on page 20
5. change R380,R379,R381 form 0805 to 0603 page 20
6. Add R94,R87 Vender suggesttion on page 21
7. Analog ground change to digital ground on page 21
8. reserve C5,C6,C883,C884 on page 22
9. reserve +3VALW on page 22
10.change +3VS to +CAM_VCC on page 22
11.change R651,R634 form (0_0603) to 43 x 39 jump on page 23
12.add net name +3VS_READER on page 23
13.add net name AV_PLL on page 23
14.add net name VREG on page 23
15.+3VS change to +3VS_READER on page 23
16.change R619 BOM structure on page 23
17.add net name RREF on page 23
18.del R623(0_0402) on page 23
19.Chang C855 form 4.7U to 10U on page 24 vendor suggest
20.Chang C846 form 4.7U to 10U on page 24 vendor suggest
21.change BJT form MMJT9435T1G to MBT35200 on page 24
22.change EC signal name form BT_OFF# to BT_ON# on page 25
23.change D12,R103,R104 BOM structure on page 25
24.change J1,J3(43 x 79) to R186,R193(0_0805) on page 26
25.change Q3 from 2N70002_SOT23 to 2N7002W-T/R7_SOT323-3 on page 26
26.change Q1 form 2N70002_SOT23 to 2N7002W-T/R7_SOT323-3 on page 26
27.change net name form WWAN_LED# to WWAN_LED_R# on page 28
28.change R130 BOM structure on page 28
29.change JP3 pin assignment on page 28
30.change Q2,Q15,Q24,Q7,Q23 form 2N70002_SOT23 to 2N7002W-T/R7_SOT323-3 on P29
31.change R18,R169,R280,R61,R279,Q2,Q15,Q24,Q7,Q23 BOM structure on age 29
32.+5VALW CHANG TO VL on page 29

- <2008/11/17>
1. update POW SCH
2. change DIMMA from H5.2 to H4 on page 11
3. change +3VS to +5VS on page 14
4. change J9,J10,J11 from 43x39 to 43x79 on page 19
5. change R563,Q31 BOM structure on page 13
6. del +3VALW on page 22
7. del +1.5VS,+VCCP,+0.9VS,+1.8V Discharge
 path R18,R280,R61,R279 Q2,Q24,Q7,Q23 on page 29
8. change R24 BOM structure on page 17
9. del R253 on page 19
10.change L14 to R382 on page 25

- <2008/11/17>
1. ADD WWAN_WAKEUP# ON pin 45 on page 19
2. DEL R79 ,R92 and change net name to WWAN_WAKEUP# on page 25
3. DEL R90 and WWAN_LED_R# on pin 85 on page 25
4. change net name form WWAN_LED_R# to WWAN_LED# on page 28

- <2008/11/18>
1. Place R282,R296 close to F27,D27 on page 8
2. Del R93 R407(0_0402) on page 19
3. Move R204 from P16 to P25
4. Move R24 from P17 to P25
5. change Q10A,Q10B to 0 ohm on page 12
6. del pull up resistance (R112,R108) on page 12
7. change C883 from 4.7u to 10u on page 22

- <2008/11/20>
1. change R112,R108,Q10A,Q10B BOM structure on page 12
2. add R149,R150 on page 12
3. add pull up resistance R292 on page 19
4. del R66(0_0402),R67(10K_0402) on page 25
5. restore R563,Q31 BOM structure on page 13
6. change D25 BOM structure on page 20

- <2008/11/21>
1. Change +3VS to +3VALW on page 19
2. del R204 on page 25
3. del R143 and CLK_SD_48M on page 12
4. Change R137 from 12 ohm to 33 ohm on page 12
5. Move Card Reader to small board on page 23
6. Move SATA HDD Conn to small board on page 22
7. ADD JP7 on page 22
8. change JP2 from 6 pin to 8 pin on page 26
9. DEL LID Switch on page 26

- <2008/11/24>
1. return the H5.2 pootprint on page 11

- <2008/11/25>
1. add add R90 on page 19
2. change JMIN1 Conn printfoot on page 19
3. change JP2 Conn on page 26
4. change JP13 Conn on page 28
5. update power SCH

- <2008/11/26>
1. change JP20 Conn and pin design on page 21
2. change JBT1 form 8 pin to 4 pin on page 19
3. del JP1 on page 13
4. SWAP JP12 on page 27
5. change JLVDS1 Conn form 20 pin to 30 pin on page 13
6. Del JP4 on page 20
7. combine the DMIC Conn and Camera Conn on page 13
8. add U7 on page 28
9. del JP3 on page 28
10.ADD SATA&CARDREADER&USB Conn(JP7) on page 22
11.update Power SCH
12.change C233 BOM structure on page 19
13.change JRJ45 Conn on page 24

- <2008/11/28>
1. update Power SCH

- <2008/12/01>
1. chang JP2 Conn on page 26
2. udate Power SCH

- <2008/12/02>
1. SWAP JLVDS1 on page 13
2. del C843,C844 on page 24
3. change C847 from 0.1u to 1u on page 24
4. change C873 from 0.1u to 1u on page 24
5. move R441,R438 form P13 to P20 on page 20
6. change +SVAMP to +5VS on page 21
7. R2,R4,R518 close to EC on page 26
8. R1 close to Q3 on page 26

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